COEN-4720 Embedded Systems

Lecture 11
DAC, ADC

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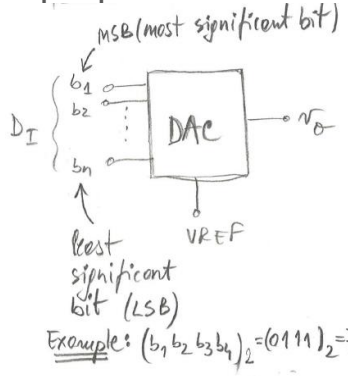
BE THE DIFFERENCE.

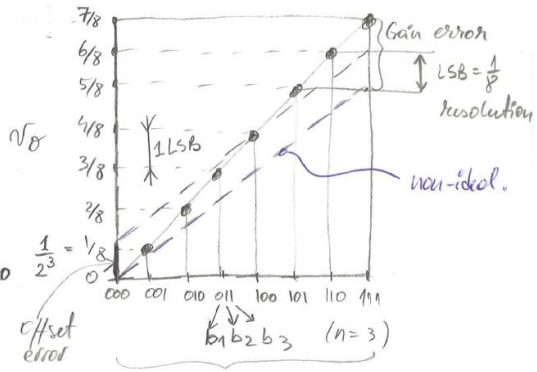
Outline

- Digital to Analog Converter (DAC)
- Analog to Digital Converter (ADC)

Digital to Analog Converter (DAC)

- DAC - device that converts a digital number to an analog signal, which is proportional to a supplied reference voltage VREF





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(1) $v_O = k V_{REF} \cdot D_I$

$= k V_{REF} \left(b_1 \cdot \frac{1}{2} + b_2 \frac{1}{2^2} + \ldots + b_n \frac{1}{2^n} \right)$ (MSB, LSB)

$= k \cdot V_{REF} \cdot \sum_{i=1}^{n} \frac{b_i}{2^i}$

Definitions:

- FSR ≡ full scale range $V_{FSR} = k V_{REF}$
- FSV ≡ full scale value $V_{FSV} = (1 - 2^{-n}) V_{FSR}$
- LSB ≡ Resolution $\frac{V_{FSR}}{2^n}$

- This is called a multiplying DAC because v_O is obtained by multiplying $V_{REF} \times D_I$: $D_I = b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \ldots + b_n \cdot 2^{-n}$

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DA Techniques

- Weighted resistor
- Weighted capacitor
- Voltage-mode R-2R ladder
- Current-mode R-2R ladder
- R-string (potentiometric)
- …

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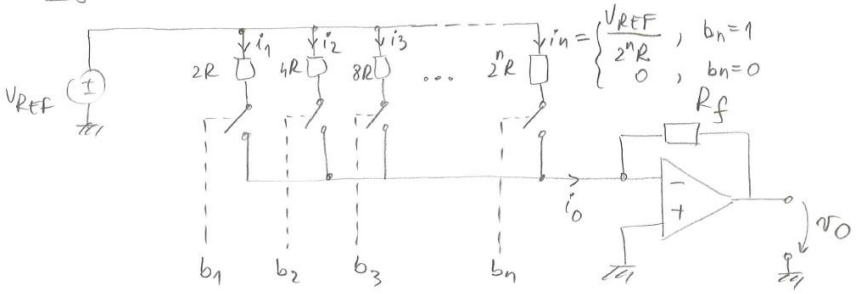
Weighted Resistor

- Drawbacks
  - Non-zero switch resistance
  - Wide spread of resistor values (exponential increase!)



$$\frac{v_O}{R_f} = -i_O$$

$$v_O = -\frac{R_f}{R} \cdot V_{REF}\left(b_1 \frac{1}{2} + b_2 \frac{1}{4} + b_3 \frac{1}{2^3} + \ldots + b_n \frac{1}{2^n}\right)$$

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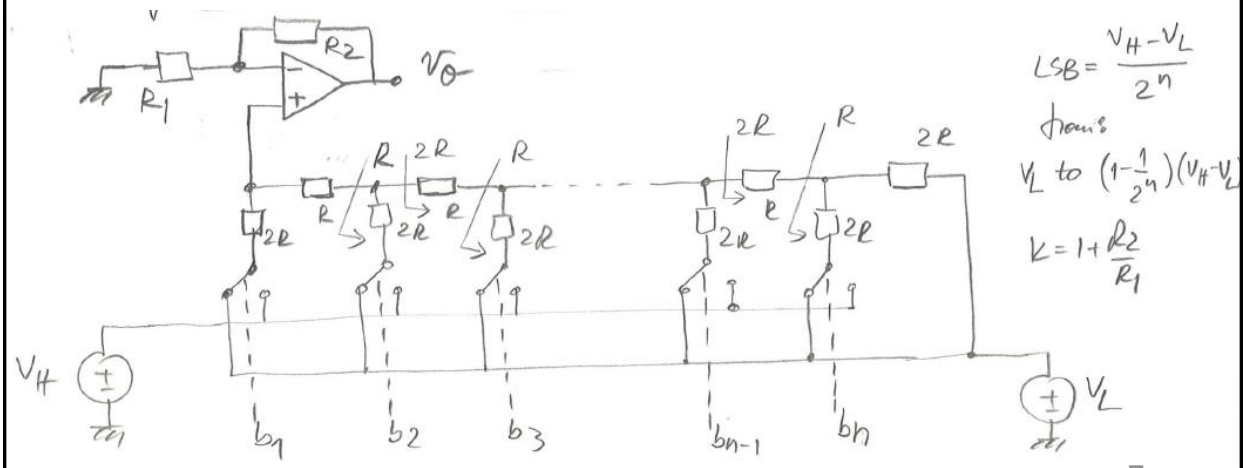
Voltage-mode R-2R Ladder

- Advantage
  - We can interpolate between any V_L and V_H



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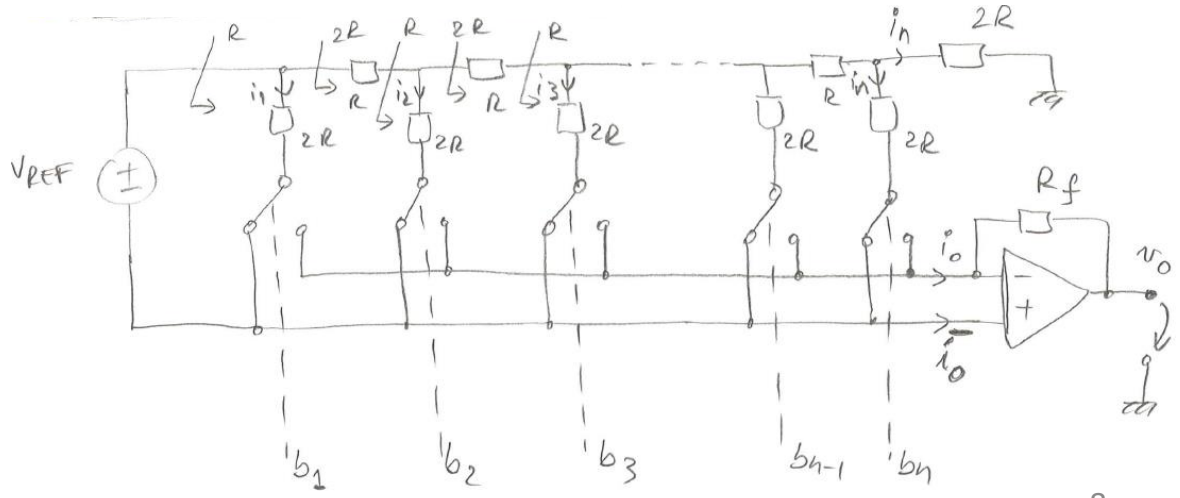
Current-mode R-2R Ladder



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$$i_1 = \frac{V_{REF}}{2R} = \frac{V_{REF}}{R}\cdot\frac{1}{2}$$

$$i_2 = \frac{V_{REF}}{4R} = \frac{V_{REF}}{R}\cdot\frac{1}{2^2}$$

$$\dots$$

$$i_n = \frac{V_{REF}}{R}\cdot\frac{1}{2^n}$$

$$\frac{v_0}{R_f} = -i_0$$

$$v_0 = -R_f \cdot i_0$$

OBS:- Note that $i_0 + \bar{i}_0 = (1-2^{-n})\cdot\frac{V_{REF}}{R}$ regardless of $D_I = b_1 b_2 b_3 \dots b_n$!

- $\bar{i}_0$ is said to be complementary to i_0

$$v_0 = -\left(\frac{R_f}{R}\right) V_{REF}\cdot\left(b_1\frac{1}{2} + b_2\frac{1}{2^2} + \dots + b_n\frac{1}{2^n}\right)$$

$$\triangleq K = -\frac{R_f}{R}$$

$$v_0 = K V_{REF}\left(b_1\frac{1}{2} + b_2\frac{1}{2^2} + \dots + b_n\frac{1}{2^n}\right)$$

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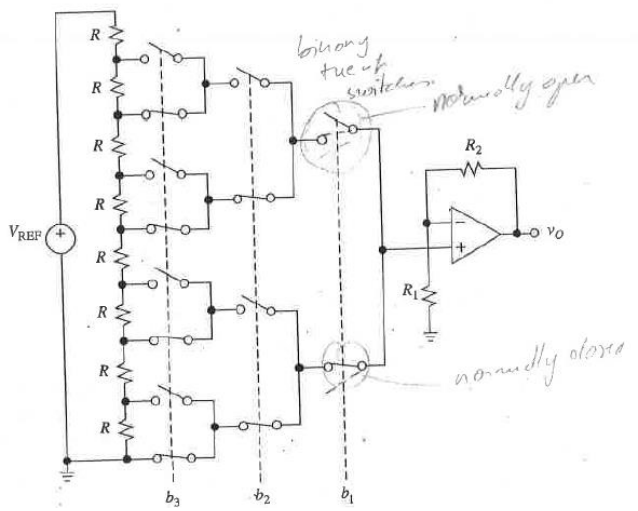
R-string (Potentiometric) Architecture



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R-string Architecture

- Advantages
  - Simple; needs only identical resistors
  - Fast for less than 8-10 bits
  - Low-power
  - Compatible with purely digital technologies
- Disadvantages
  - 2^n resistors and 2^n switches – high area and power
  - High settling time for n>10

STM32L053R8 MCU

15 Digital-to-analog converter (DAC)

15.1 Introduction

The DAC module is a 12-bit, voltage output digital-to-analog converter. The DAC can be configured in 8- or 12-bit mode and may be used in conjunction with the DMA controller. In 12-bit mode, the data could be left- or right-aligned. An input reference voltage, V_{REF+}(shared with ADC), is available. The output can optionally be buffered for higher current drive.

15.2 DAC1 main features

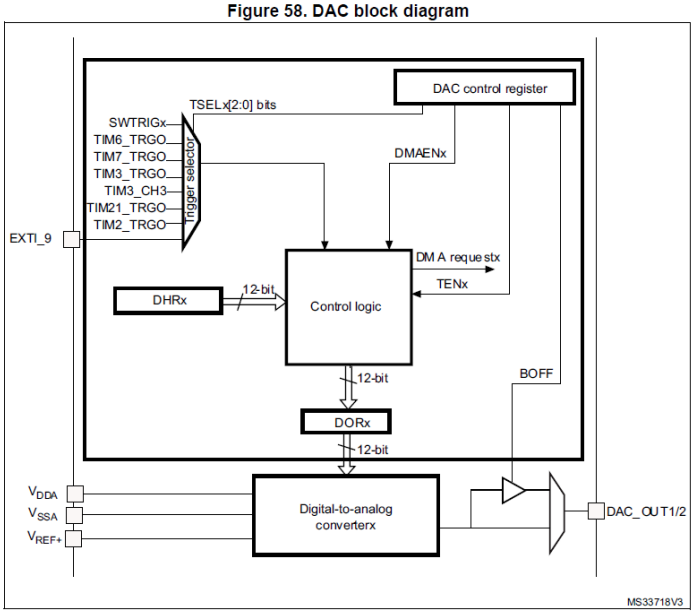
The devices integrate two DAC converters, featuring one output channel each: DAC_OUT1 and DAC_OUT2.

DAC1 main features are the following:

- One data holding register
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- DMA capability (including underrun detection)
- External triggers for conversion
- Input voltage reference, V_{REF+}

Source: MCU Reference Manual

Figure 58. DAC block diagram



Source: MCU Reference Manual

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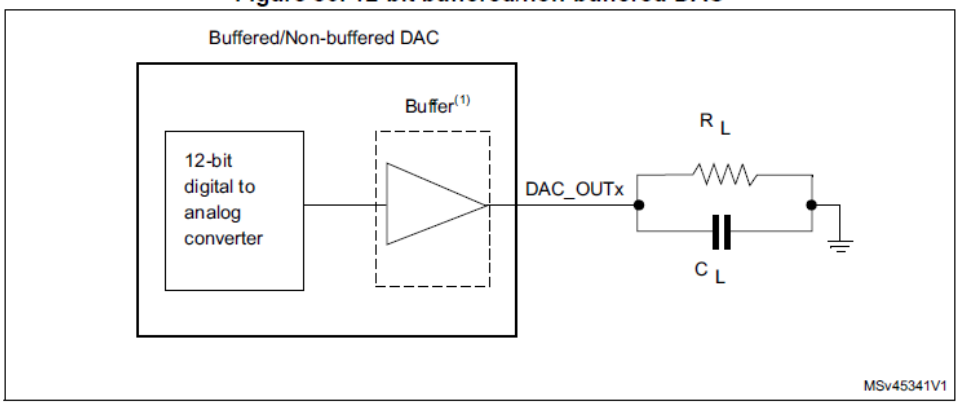
Figure 30. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Source: MCU Datasheet

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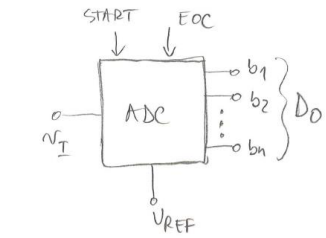
Outline

- Digital to Analog Converter (DAC)
- Analog to Digital Converter (ADC)

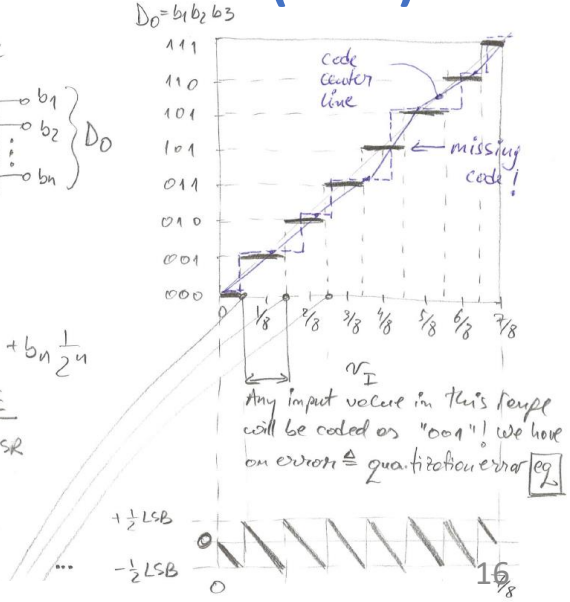
Analog to Digital Converter (ADC)

- ADC: provides the inverse function of DAC!



$$D_O = b_1\frac{1}{2} + b_2\frac{1}{2^2} + \dots + b_n\frac{1}{2^n}$$

$$= \frac{V_I}{k \cdot V_{REF}} = \frac{V_I}{V_{FSR}}$$



AD Techniques

- Charge redistribution converters
- Subranging converters
- Integrating-type converters
- Flash converters
- DAC based AD conversion (successive approximation register based converters)
- …

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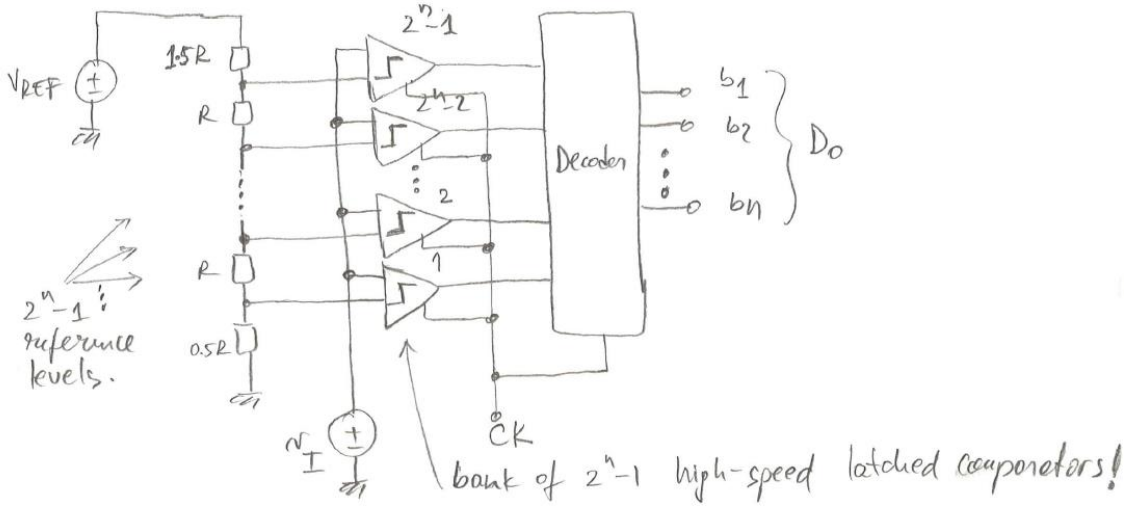
Flash converters



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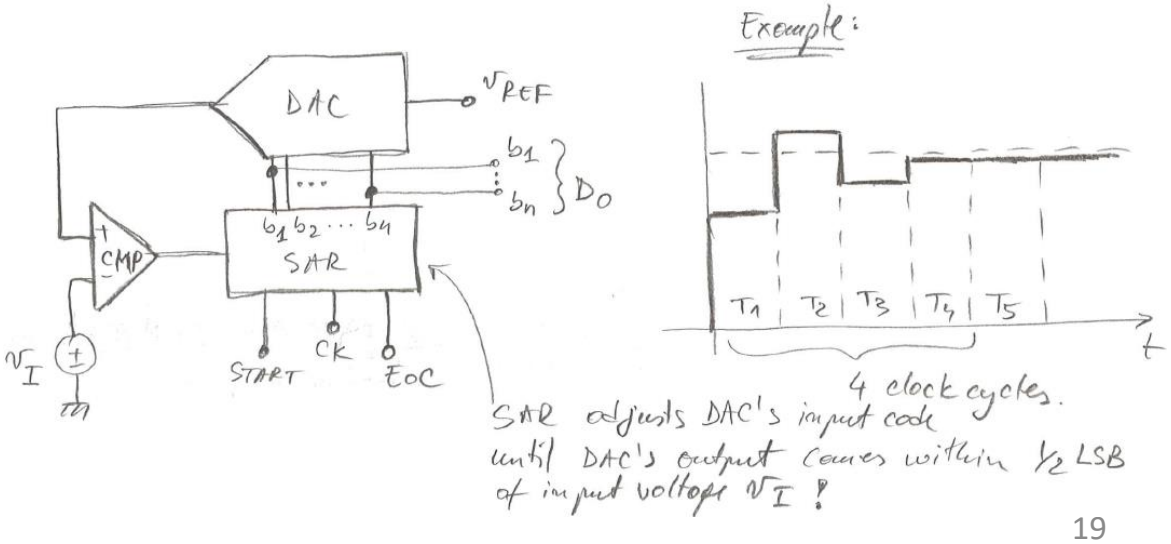
DAC based AD conversion



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14 Analog-to-digital converter (ADC)

14.1 Introduction

The 12-bit ADC is a successive approximation analog-to-digital converter. It has up to 19 multiplexed channels allowing it to measure signals from 16 external and 3 internal sources. A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency.

A built-in hardware oversampler allows analog performances to be improved while off-loading the related computational burden from the CPU.

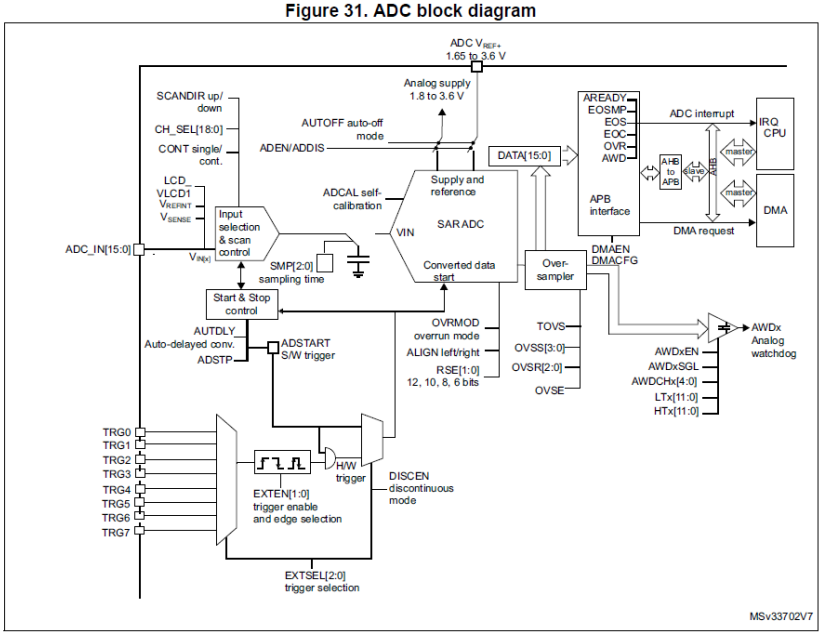
Source: MCU Reference Manual

14.2 ADC main features

- High performance
  - 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
  - ADC conversion time: 0.87 µs for 12-bit resolution (1.14 MHz), 0.81 µs conversion time for 10-bit resolution, faster conversion times can be obtained by lowering resolution.
  - Self-calibration
  - Programmable sampling time
  - Data alignment with built-in data coherency
  - DMA support

Source: MCU Reference Manual

Figure 31. ADC block diagram



Source: MCU Reference Manual

References

- Sergio Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, McGraw Hill, 3rd edition, 2003.

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