Senior Design Project Proposal

Department of Electrical and Computer Engineering, Marquette University
Cristinel Ababei
cristinel.ababei@marquette.edu

1. Project Title: uDetectFace: Development of a face detection algorithm on an FPGA

2. Project Description:

The goal of this project is to implement a face detection algorithm on an FPGA (field programmable gate array). Such an implementation would be able to process realtime video streams much faster than conventional software only approaches. By implementing the detection algorithm on an FPGA, we can take advantage of the available parallelism offered by the available logic of the FPGA. Thus, the FPGA serves as a hardware accelerator of the face detection algorithm. We will implement the popular Viola-Jones detection algorithm.

3. Project Design Objectives:

The following are the main steps.

1. Study Viola-Jones algorithm for face detection. We'll start with an existing all software implementation (C/C++ or Matlab).
2. Write the VHDL/Verilog code in order to implement the detection algorithm on an FPGA chip. We'll use an Altera FPGA chip on an existing FPGA development board.
3. Use Quartus II Web Edition to synthesize the design and deploy it onto the FPGA chip.
4. Test the prototype system on real videos streams from a camera attached to the FPGA board or from the host computer.
5. Maintain a project website.

4. Project Prerequisites:

Experience with programming in VHDL/Verilog and working with FPGA boards. Familiarity with FPGA CAD tools, such as Altera's Quartus II Web Edition or Xilinx's ISE WebPack. Basics of image/video processing. Knowledge of C/C++ or Matlab is desired. Past experience with hardware prototyping is a plus. Most importantly, students should be self-motivated to learn new interdisciplinary approaches that bridge knowledge and skills from digital design, FPGAs, VHDL/Verilog and C/C++ programming, and image/video processing.