ECE-470 – Digital Design II Introduction

Overview

- Class:
  - Time: 2:00-3:15PM TuTh
  - Location: ECE-243
  - Credits: 3
  - Web page: http://venus.ndsu.nodak.edu/~cris/ece470
- Text: Essentials of Electronic Testing for Digital Memory and Mixed-Signal VLSI Circuits, M. Bushnell, V. Agrawal, Springer 2000.
- Grades:
  - 20% Homework
  - 30% Projects (Project 1: 15%, Project 2: 15%)
  - 15% + 15% Midterms 1,2
  - 20% Final exam

Office Hours

- Cristinel Ababei
  - Email: cristinel.ababei (at) ndsu.edu
  - Phone: (701) 231-7617
  - Office: ECE-101F

  - Office hours: 10:00-11:30am TuTh

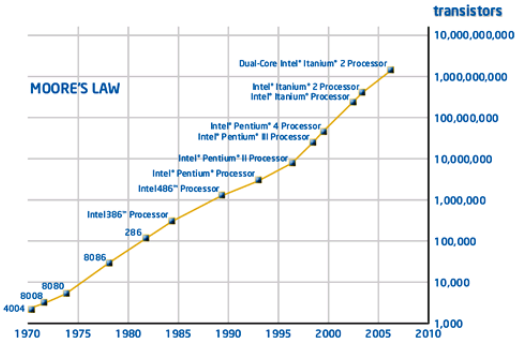
This Course

- Bulletin description:
  - "Design and analysis of reliable digital systems through robust information coding, fault avoidance, and fault tolerance"
- Prerequisites
  - ECE-275, ECE-375
  - Knowledge of C++, VHDL for projects
- What is different from "Digital Design I"?
  - Emphasis on testing, fault simulation, test generation, testable design, design for testability
  - Class projects
  - Has CAD (algorithm implementation) aspect in first part

This Course

VLSI CAD	Digital Design	Analog, Mixed, Others
ECE 7xx Design Automation	ECE 275 Digital Design I	ECE 375 Digital System Design, VHDL
	ECE 423/623 Digital VLSI Design	ECE 424/624 Analog VLSI Design
	ECE 470/670 Digital Design II	ECE 723 Advanced Electronics
	ECE 471 Computer Systems Design, FPGAs	

Transistor Count Annual Growth



Present and Future*

	1997 -2001	2003 - 2006
Feature size (micron)	0.25 - 0.15	0.13 - 0.10
Transistors/sq. cm	4 - 10M	18 - 39M
Pin count	100 - 900	160 - 1475
Clock rate (MHz)	200 - 730	530 - 1100
Power (Watts)	1.2 - 61	2 - 96

* SIA Roadmap, *IEEE Spectrum*, July 1999

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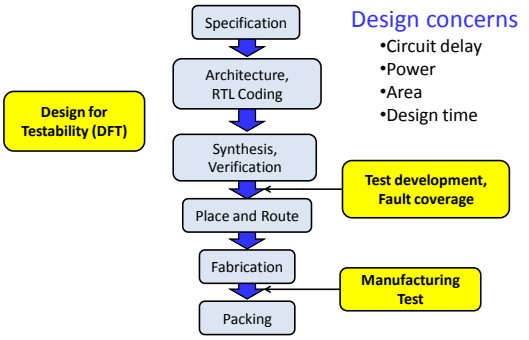
VLSI Implementation Flow



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Verification Vs. Testing: Definitions

- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure correctness of the synthesized design; when manufactured, will perform the given I/O function.
- Test: Manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

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Verification Vs. Testing

- Verifies correctness of synthesized design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  - 1. Test generation: software process executed once during design
  - 2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

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Need for Testing

- Functionality issue
  - Does the circuit work?
- Density issue
  - Higher density → higher failure probability
- Application issue
  - Life critical applications
- Maintenance issue
  - Need to identify failed components
- Cost of doing business
- What does testing achieve?
  - Discard only the "bad product"?

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Testing Cost

- Software processes of test
  - Fault simulation and test generation
  - Test programming and debugging
- Design for testability (DFT)
  - Chip area overhead and yield reduction
  - Performance overhead
- Manufacturing test
  - Automatic test equipment (ATE) capital cost
  - Test center operational cost
- Increases with circuit size/complexity
- Increases 10X at each higher level

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Cost of Manufacturing Testing (2000)

- 0.5-1.0GHz, analog instruments,1,024 digital pins: ATE purchase price
  = $1.2M + 1,024 x $3,000 = $4.272M
- Running cost (five-year linear depreciation)
  = Depreciation + Maintenance + Operation
  = $0.854M + $0.085M + $0.5M
  = $1.439M/year
- Test cost (24 hour ATE operation)
  = $1.439M/(365 x 24 x 3,600)
  = 4.5 cents/second

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Levels of Testing

- Levels
  - Chip
  - Board
  - System
  - Boards put together
  - System-on-Chip (SoC)
  - System in field
- Rule of 10: It costs 10 times more to test a device as we move to higher level in the product manufacturing process

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Levels of Testing

- Other ways to define levels – these are important to develop correct "fault models" and "simulation models"
  - Transistor
  - Gate
  - RTL
  - Functional
  - Behavioral
  - Architecture
- Focus in this course: Chip level testing – gate level design

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Role of Testing

- Detection: Determination whether or not the device under test (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- Failure mode analysis (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

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Overview

- PART 1: Test generation
  - Test economics, Fault models, Fault simulation, Combinational, sequential ATPG, Memory test, IDDQ test.
- PART 2: Design for testability (DFT)
  - DFT refers to hardware design styles or added hardware that reduces test generation complexity.
  - Scan design, BIST.
  - System test

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