An 88% Efficiency 0.1–300-μW Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes

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***Abstract*— This paper presents a novel 3-D maximum power point tracking (3-D MPPT) system for energy harvesting systems (EHS) within Internet of Things (IoT) smart nodes. The proposed 3-D MPPT utilizes a switch width modulation (SWM) technique for improving power efficiency (PE) at idle (<1 μA) and heavy (>300 μA) load modes. The SWM eliminates the gate driver/conduction loss tradeoff in a reconfigurable switched capacitor charge pump (SCCP). The proposed SWM technique modulates the SCCP switch resistance in proportion to the load condition, input voltage, and V_{gs} applied. A cold startup technique is incorporated in the proposed EHS with an energy-aware algorithm for input harvester select purpose. The fabricated test chip in 65-nm CMOS technology can harvest solar and thermal energy from 0.35 V and provides a regulated output voltage at 1 V with the peak efficiency of 88% at 200 μW and PE >60% at 100 nW.**

***Index Terms*— Energy harvesting system (EHS), Internet-of-Things (IoT), maximum power point tracking (MPPT), photovoltaic (PV) cells power management circuits (PMS), thermoelectric generator (TEG).**

I. Introduction

FOLLOWING the international technology roadmap of semiconductor and the recent advances in integrated circuits technology, Internet of Things (IoT) smart nodes, including wearable devices, wireless electronics, and implantable sensors proliferate and increasingly become popular. The smart nodes within IoT applications will reach nearly 50 billion connected devices by 2020 [1]–[5]. These smart nodes are usually implemented as IoT SoC and includes power management circuit (PMC), energy sources, signal processing, communication blocks, and sensors and/or actuators, as illustrated in Fig. 1. Power efficiency (PE), small silicon area, and cost efficiency are the main challenges for IoT SoC implementation. Hence, fully integrated, self-adaptive, and cost-efficient PMC design becomes crucial within IoT smart nodes. In this aspect, energy harvester powered PMC garners a considerable attention as it features energy-autonomous IoT smart nodes, and avoid the maintenance cost of recharging and/or replacement of batteries and their bulky size [1], [2], [5]–[10].

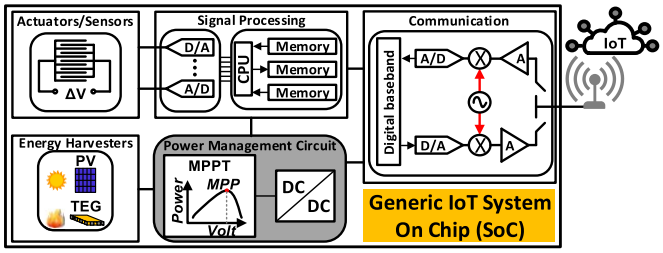

Fig. 1. Generic IoT SoC with dc EHS.

Numerous energy harvesters have been studied and discussed in the literature, including photovoltaic (PV) [1], [4], [9], [12]–[15], thermoelectric generators (TEG) [16]–[18], and piezoelectric [19].

Among these energy scavengers, PV has gained a significant attention and popularity as an energy source for autonomous IoT SoC due to its high-power density and low cost [3]. The solar energy can be harvested using inductive-based [5], [17], [22], [23] or switched capacitor-based dc–dc converter [1], [3], [4], [6], [7], [11], [14], [15]. However, the latter is a more suitable solution for fully integrated IoT SoC, such as smart nodes and body-area-network (BAN), avoiding bulky OFF-chip inductors. To maximize the solar energy being harvested, PV is connected to a switched capacitor dc–dc converter controlled by a maximum power point tracking (MPPT). The MPPT makes the system operate at its maximum efficiency point (i.e., harvesting and conversion efficiency). The need of MPPT, along with the dc–dc converter rises from the harvester nature dependence and load power variability, especially at a regulated output voltage. In this aspect, the MPPT can have two roles within an energy harvesting systems (EHS) [21]: 1) conditioning the harvester output to a suitable dc level in order to maximize the scavenged energy from the harvester and/or 2) controlling the dc–dc converter to maximize the converted amount of energy harvested at the input to the output as per load demand (i.e., balancing the load/harvested-power operating point for maximum conversion efficiency). It should be noted that the dc–dc converter can be controlled either to harvest the power demanded by the load or to harvest maximum power

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available from the transducer and store it in a buffer [21]. The proposed 3-D MPPT focuses on the second role of the MPPT within an EHS to improve the modest conversion efficiency achieved by the prior arts at light loads, and to improve it further at heavy loads, as explained in the next paragraph.

Many hill-climbing-based MPPT principles have been exploited to maximize the converted harvested power as per load demand. Although they achieve a considerable PE (i.e., conversion efficiency) at 100 s of microampere output load, they suffer from a modest PE (30% – 40%) when supplying 100 s of nanowatt load during idle mode. Wu *et al.* [5] mentioned that the IoT sensor nodes operation profile stays more than 50% of its operation time in idle mode. Moreover, Lee *et al.* [24] show a wireless operation scenario, that proves the former claim. It shows that the IoT wireless sensor wakes up only during the heavy-duty functions and operates most of the time in idle or standby mode. According to Wu *et al.* [5], a typical wireless sensor node wakes up once every 60 s, or even more, thus, the conversion efficiency during the idle and standby (i.e., light load) mode dominates the overall PE of the EHS. Therefore, high PE at ultra-light loads (i.e., 100 s of nanoampere) is crucial to avoid the degradation of the EHS PE within IoT smart nodes and implantable sensors.

Conventionally, the hill-climbing-based MPPT reported in the literature utilizes conversion ratio modulation (CRM) and/or switching frequency modulation (SFM) techniques limiting their MPPT process to one or two dimensions. The 1-D MPPT was adopted in [4] and [7] by tuning the switching frequency ($f_{\rm sw}$) and the pumping capacitor values, respectively. Although the high efficiency achieved, the associated PE is limited to 40% at light load (<1 μA). Moreover, the large area occupied by the capacitor bank in [4] make it less cost efficient while the lack of a reconfigurability in [4] and [7] induces charge redistribution loss (CRL), degrading the PE. The 2-D MPPT in [3] employed CRM and SFM using a hysteresis control technique to achieve a peak PE of 89%. However, as the output load goes below 1 μA, the PE decreases to less than 50%. The PE limitation of the conventional MPPT is due to the fixed transistor sizes for the dc–dc converter across a wide load range.

In this paper, a reconfigurable serial–parallel switched capacitor charge pump (SP SCCP) and a novel $V_{\rm gs}$-dependent switch width modulation (SWM) technique are incorporated into the MPPT procedure along with the SFM and CRM techniques resulting in the proposed 3-D MPPT. The proposed 3-D MPPT eliminates the gate driver/conduction loss tradeoff by configuring the SP SCCP transistor widths with proportion to the load condition and the input voltage applied. In addition, the proposed 3-D MPPT is self-adaptive and compatible with various dc energy harvester types such as PV and TEG.

The remainder of this paper is organized as follows. The proposed 3-D MPPT along with the SWM operation principles are discussed in Section II. Section III explains the architecture and the circuit implementation of the proposed 3-D MPPT. The startup technique, the energy-aware algorithm, and the 3-D MPPT closed-loop operation are presented in Section IV, followed by the measurement results in Section V. Finally, Section VI concludes this paper.

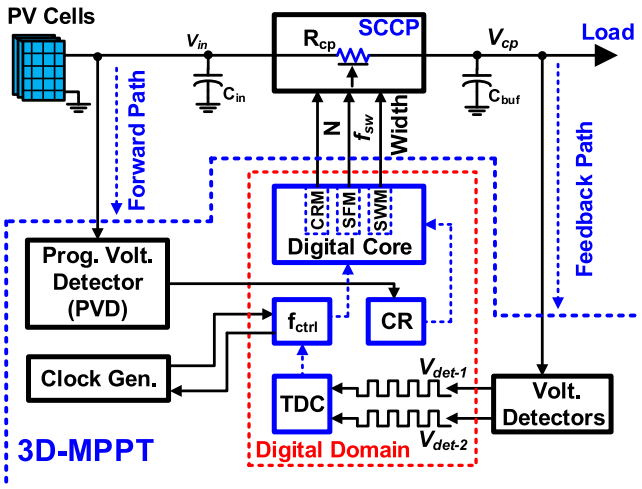

Fig. 2. Proposed 3-D MPPT behavioral diagram for PV cells.

II. Proposed 3-D MPPT Operation Principle and Algorithm

The main idea of the hill-climbing MPPT is to condition the dc–dc converter equivalent input impedance ($R_{\rm cp}$) to minimize the internal losses and maximize the power transfer to the load. In that aspect, the proposed 3-D MPPT also employs a hill-climbing MPPT concept assisted with several techniques to improve the PE across a wide output load range. This section discusses the proposed 3-D MPPT tracking principle followed by the proposed SWM technique for a further PE improvement.

A. 3-D MPPT Tracking Principle

Fig. 2 describes the proposed 3-D MPPT behavioral diagram. The $I_{\rm load}$ condition is sensed by analyzing the voltage detectors (VDs) output pulses ($V_{\rm det-1}$, $V_{\rm det-2}$) through a feedback path. While the $V_{\rm in}$ range is detected using a programmable VD (PVD) through a forward path. A simple time-to-digital converter (TDC) and two digital registers [$f_{\rm ctrl}$ and reconfiguration register (CR)] are developed so that $I_{\rm load}$ condition and $V_{\rm in}$ detected range can be digitally stored. Then, a digital core sets "$f_{\rm sw}$" and the conversion ratio "N" using $f_{\rm ctrl}$ and CR digital values, respectively. This has two benefits. First, "$f_{\rm sw}$" and "N" can be used by the SWM technique to optimize the SCCP transistors width as indicators for $I_{\rm load}$ and $V_{\rm in}$, respectively. Second, low-complex operation and low power implementation are feasible since the SWM can be adopted in the digital domain.

In general, the tradeoff between the gate driver and the conduction loss rises at wide load applications including IoT smart nodes that demand 100 s of nanoampere to 100 s of microampere depending on the operating mode. More specifically, the SCCP internal losses including conduction loss and gate driver loss depend on the transistors width and the $f_{\rm sw}$ at a given operating condition. The PE, in this case, can be expressed as follows:

$$\mathrm{PE} = \frac{(N \times V_{\rm in} - \Delta V_d) \times I_{\rm load}}{N \times V_{\rm in} \times I_{\rm load} + P_g} \tag{1}$$

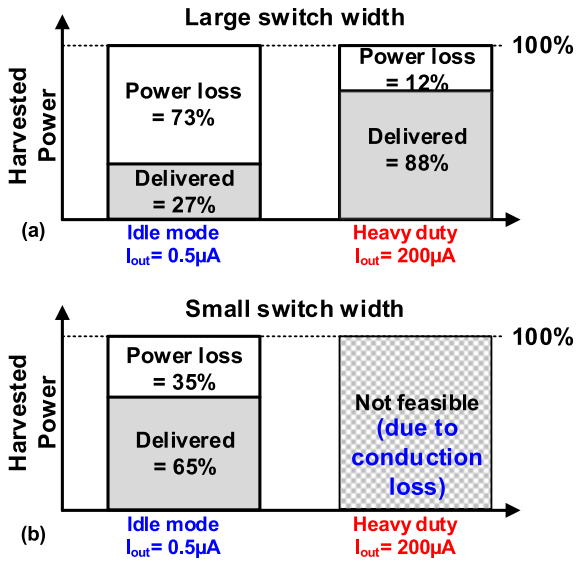

Fig. 3. Simulated power distribution of a 2× SCCP at idle and heavy operation modes with (a) large transistor width and (b) small transistor width.

$$\times \Delta V_d \propto \frac{N \times I_{\text{load}}}{1/R_{\text{cp}}} \propto \frac{N \times I_{\text{load}}}{C_{\text{fly}} \times f_{\text{sw}}} \tag{2}$$

where ΔV_d is the drop voltage across the SCCP due to conduction loss and defined by (2), C_{fly} and N are the SCCP flying capacitance and conversion ratio, respectively. P_g is the gate driver loss, and it is defined as follows:

$$P_g \propto C_{\text{sw}} V_{\text{gs}}^2 f_{\text{sw}} \tag{3}$$

where C_{sw} is the transistor gate capacitance and V_{gs}' is applied swing voltage per switch.

Fig. 3 shows a simulated 2× SP SCCP power consumption distribution at idle and heavy-duty operation modes. To analyze the PE limitation issue, a simulation is carried out assuming I_{load} equals 500 nA and 200 μA at idle and heavy-duty mode, respectively. At heavy load scenarios, P_g, in (1), is far less than $N \times V_{\text{in}} \times I_{\text{load}}$ [13], and can be neglected. In this case, PE can be improved by reducing the conduction loss that arises from the charging and discharging of C_{fly} through the SCCP switches and limited by ΔV_d. According to (2), modulating f_{sw} with I_{load} and N variations reduces ΔV_d, hence, improving the PE. For a further PE improvement, large SCCP transistors with small R_{ON} are required to minimize the R_{cp}, and hence, to reduce ΔV_d. At light load and idle conditions, P_g dominates and significantly decreases the PE. There are various means to reduce P_g. The SFM technique reduces f_{sw} with I_{load}, and hence, reduces P_g. However, the effect of this technique on the PE reduces at ultra-light load condition where P_g dominates the losses where SFM is already applied. Therefore, P_g can be further reduced by decreasing the C_{sw} associated with each SCCP transistor (i.e., small switch width), thus increasing R_{cp}.

In addition, according to (2) and (3), assuming the same V_{in}, R_{cp} requirements differ across the load range. Large SCCP transistors with small on-resistance (R_{ON}) and consequently small R_{cp} are required to maintain regulation and minimize the conduction loss at heavy load conditions. While at light load scenarios, using small transistors with large R_{ON} and reduced C_{sw} are enough to maintain regulation and reduce P_g. Therefore, the proposed 3-D MPPT employs a novel V_{gs}-dependent SWM technique together with SFM and CRM (i.e., 3-D tracking process) to improve the PE at idle and heavy load conditions. The basic idea is to modulate the implemented SCCP transistors width in proportion to I_{load} and V_{in} values, along with the f_{sw} and the "N" to minimize the internal losses, boosting the PE across wide input voltage and output load range. The proposed 3-D MPPT algorithm will be discussed in Section II-B.

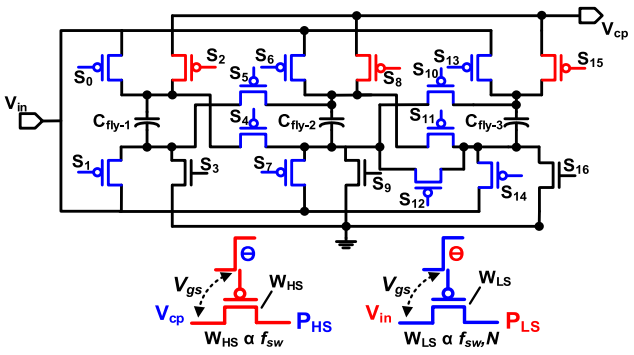

Fig. 4. SP SCCP circuit architecture.

B. V_{gs}-Dependent SWM Tracking Algorithm

The proposed SWM technique varies the SCCP transistors width (i.e., R_{ON}), and hence, R_{cp} according to the load condition to minimize the conductions loss and P_g. According to (3), P_g can be significantly reduced by an additional transistor width optimization with relative to the V_{gs} applied. In addition, the transistor R_{ON} varies with V_{gs} at the same width (W) due to the SCCP transistors linear characteristics, as follows:

$$R_{\text{ON}} \approx \frac{1}{\mu C_{\text{ox}} \left(\frac{W}{L}\right) (V_{\text{gs}} - V_{\text{th}})}. \tag{4}$$

Utilizing this information for MPPT, the proposed SWM technique optimizes the SCCP transistors width (i.e., R_{ON}) proportionally with: 1) I_{load} and 2) applied V_{in} which determines V_{gs}.

Since the SWM optimization depends on V_{gs} per each transistor, the SP SCCP switches shown in Fig. 4 are divided into two types: 1) low-side transistors (P_{LS}), with V_{gs} almost equals V_{in} and 2) high-side transistors (P_{HS}) with V_{gs} equals V_{cp}, which is regulated and equals 1 V. Thus, the P_{LS} size (W_{LS}) is modulated in proportion to f_{sw} together with V_{in}, while P_{HS} size (W_{HS}) is proportionally modulated with f_{sw} only, due to its constant V_{gs}. Following the flowchart in Fig. 5, f_{sw} and N are stored digitally into 6-bit f_{ctrl} and 3-bit CR signals, respectively. Initially, CR and f_{ctrl} are loaded with their initial values. First, if the indirectly sensed I_{load} is increasing, the 3-D MPPT algorithm increments f_{ctrl} and proportionally widens P_{LS} and P_{HS}. Likewise, when I_{load} decreases, indicating a lighter load demand, the 3-D MPPT algorithm decrements f_{ctrl} and proportionally decreases the P_{LS} and P_{HS} width.

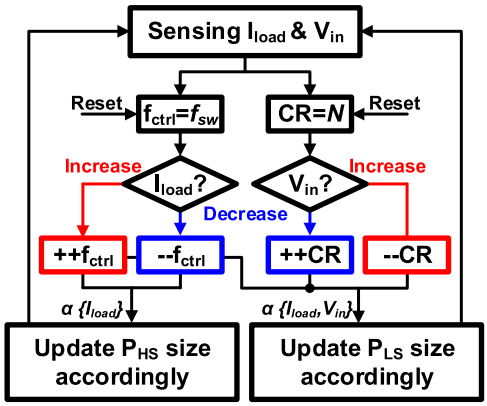

Fig. 5. Proposed 3-D MPPT flowchart.

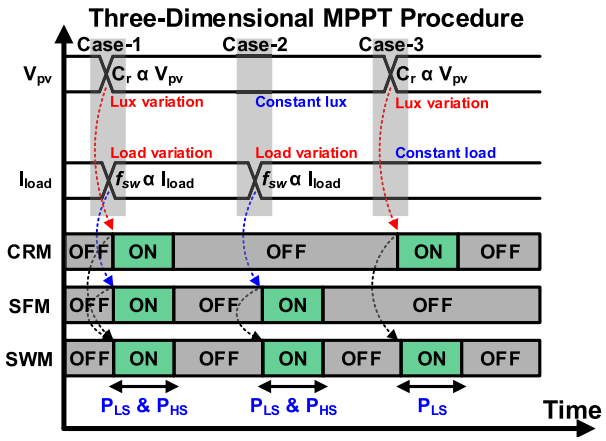

Fig. 6. Proposed 3-D MPPT operation at different operation cases.

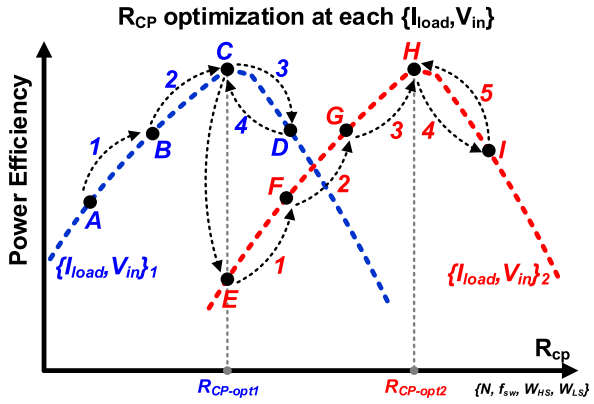

Fig. 7. 7. 3-D MPPT tracking for R_{cp} optimization per operating point {I_{load}, V_{in}}.

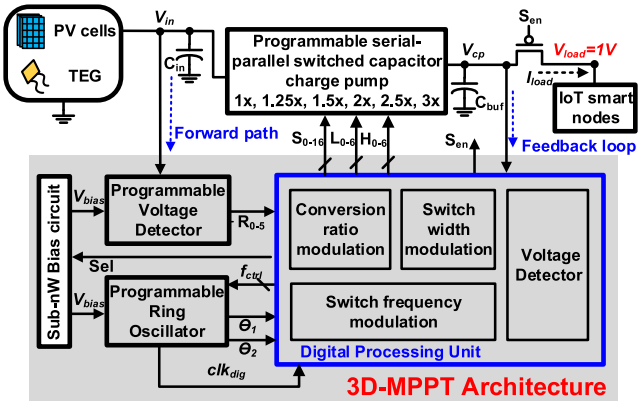

Fig. 8. Proposed 3-D MPPT system architecture.

Second, to maintain regulation and low CRL, CR is modulated inversely with V_{in} for a regulated V_{cp} equals 1 V. As shown in Fig. 5, f_{ctrl} and CR are used to update the P_{LS} size, while P_{HS} size is updated only according to f_{ctrl}. Thus, the proposed SWM technique is triggered simultaneously with CRM (case-3), SFM (case-2), or both (case-1), as described in Fig. 6.

In conclusion, the proposed 3-D MPPT track the MPP by conditioning R_{cp} using N (CRM), f_{sw} (SFM) and [W_{HS}, W_{LS}] (SWM) at each operating point defined by the pair {I_{load}, V_{in}}. Fig. 7 illustrates the proposed 3-D MPPT tracking process at two different operating points {I_{load}, V_{in}}$_{1/2}$. Initially, at {I_{load}, V_{in}}$_1$, the optimum R_{CP} ($R_{cp-opt1}$) is tracked by adjusting: 1) "N" according to the detected V_{in-1} and 2) "f_{sw}" according to the indirectly sensed I_{load-1}. Then, W_{LS} and W_{HS} are updated in proportion to the adapted N and f_{sw}(A–D in Fig. 7). At point "D" in Fig. 7, the tracking algorithm realized a decrease in PE by analyzing $V_{det-1/2}$, so it locks the MPPT process at "C". When the operating point varies to {I_{load}, V_{in}}$_2$, $R_{cp-opt2}$ is tracked from the last achieved R_{cp-opt} as shown in Fig. 7 (C–H) without the need of re-tuning the f_{sw} or N as in [3], making the tracking response faster. The TDC is employed using digital counters and edge detectors, while the PVD detects V_{in} range without the need of any reference voltages, make it an adequate solution for selfsustained, autonomous, and low-power EHS within IoT smart nodes. A detailed study of the 3-D MPPT architecture including the I_{load} indirect sensing process and the TDC will be presented in Section III.

III. Proposed 3-D MPPT Architecture and Circuit Implementation

Fig. 8 illustrates the proposed EHS along with the novel 3-D MPPT architecture. The proposed EHS harvests solar energy to provide a regulated output voltage (1 V). It is composed of a forward path and a feedback path. The forward path features a continuous V_{in} range detection to set the proper SP SCCP conversion ratio. The feedback monitors I_{load} to establish the SP SCCP f_{sw}, W_{HS}, and W_{LS} accordingly. The proposed 3-D MPPT shown in Fig. 8 consists of five main blocks, namely, a reconfigurable SP SCCP, the digital processing unit (DPU) where the proposed 3-D MPPT tracking algorithm runs, PVD to detect the V_{in} range, ultra-low-power 4 transistors (4T) reference circuits, and finally a programmable ring oscillator (PROSC) to generate clock signal for the DPU, SP SCCP, and PVD.

A. Serial–Parallel Switched Capacitor Charge Pump

To accommodate a wide input range, a reconfigurable SP SCCP is developed (Fig. 4). By manipulating the SP SCCP

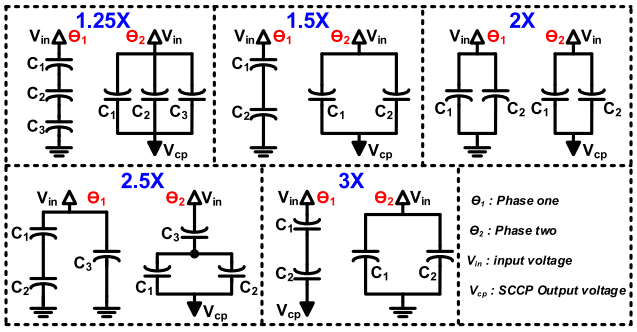

Fig. 9. SP SCCP configuration at each conversion ratio (N).

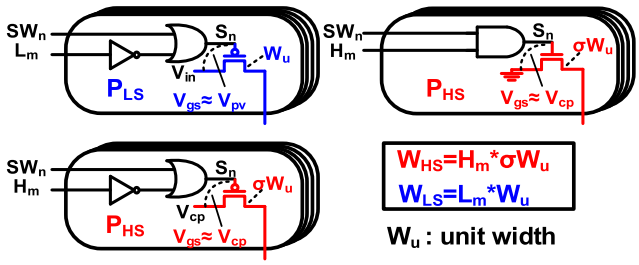

Fig. 10. SP SCCP transistors segmentation for P_{HS} and P_{LS}.

configuration using S_{0-16}, the implemented SP SCCP can boost V_{in} with six different N: 1×, 1.25×, 1.5×, 2×, 2.5×, and 3×. The SP SCCP configuration at each N is shown in Fig. 9. The CRM sets the proper N according to the detected V_{in} range using the PVD. The SP configuration for V_{in} boosting can provide multiple N with a fewer number of C_{fly}, making it an adequate solution to cover a wide input range with low silicon area. Fig. 10 shows the P_{HS} and P_{LS} segmentation architecture. P_{HS} and P_{LS} are divided into smaller transistors connected in parallel. The total width of P_{HS} (W_{HS}) and P_{LS} (W_{LS}) is defined by the digital control signals H_{0-6} and L_{0-6}, respectively, (Fig. 10). Since V_{cp} is greater than V_{in}, W_{HS} is less than W_{LS} by a proportional fraction "σ". The sizes of the control logic gates in Fig. 10 are almost minimum with low switching rates. Thus, the gate driver loss introduced by these logic gates (P_{gs}) can be neglected compared with the one added by the converter switches. For this reason, P_{gs} is omitted in the denominator in (1).

B. Digital Signal Processing Unit (DPU)

Fig. 11 illustrates the DPU architecture. It consists of three main control blocks that execute the proposed 3-D MPPT algorithm, namely, CRM, SFM, and SWM control.

1) CRM Control: The CRM control block utilizes a 6-bit digital signal (R_{0-5}) received from the PVD, holding the V_{in} range information. Then, it is encoded and stored in a 3-bit CR (Fig. 2), as explained by the timing diagram depicted in Fig. 12(a). The SP SCCP switch configuration (S_{0-16}) depends on the digital value stored in CR to set a proper conversion ratio, avoiding CRL, and hence, improving the PE across a wide V_{in} range.

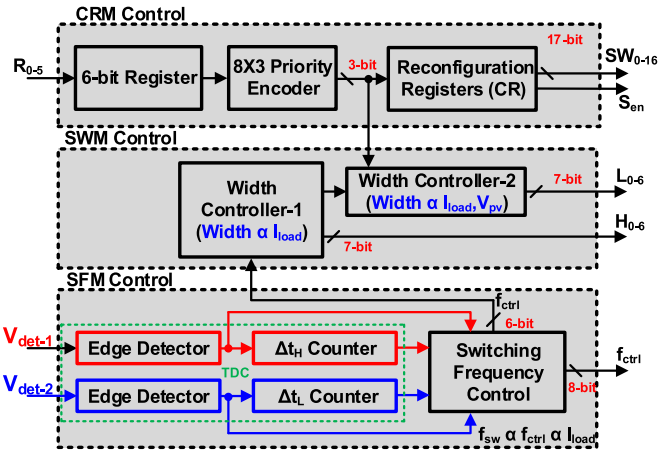

Fig. 11. DPU with SFM, CRM, and SWM control block diagram.

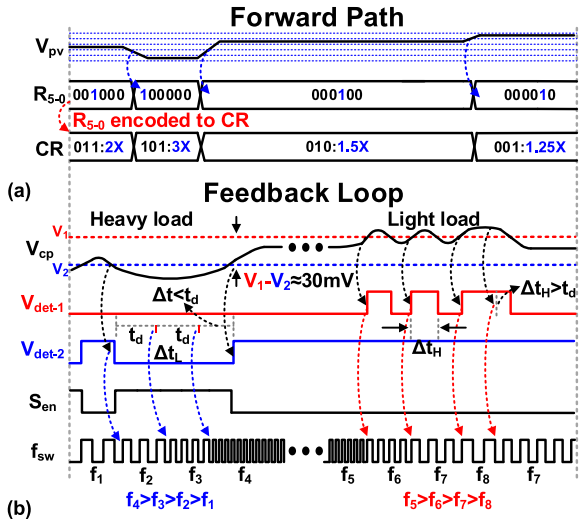

Fig. 12. Timing diagram for the DPU with (a) forward path and (b) feedback loop.

2) SFM Control: The SFM control adopts a newly event-time-driven technique responsible for sensing I_{load}, setting f_{sw}, and maintaining regulation. The proposed SFM technique is developed using two VDs that keep V_{cp} regulated between V_1 and V_2 [30-mV window] ($V_2 < V_{cp} < V_1$), a TDC to identify I_{load} condition and a PROSC to generate f_{sw} proportionally. Following the timing diagram in Fig. 12(b), at heavy I_{load} demand, f_{sw} increments one step per each V_{det-2} negative edge (event driven), demonstrating a V_{cp} droop ($V_{cp} < V_2$). However, a one-step increase may not be enough in case of a large I_{load} step. Thus, a TDC is employed to further increase f_{sw} "$\Delta t_L/t_d$" steps if the V_{det-2} low time (Δt_L) exceeds a predefined time (t_d) (time driven). In like manner, f_{sw} decrements per each V_{det-1} positive edge (i.e., $V_{cp} > V_1$) indicating lighter load condition (event driven). However, if V_{det-1} high time (Δt_H) exceeds t_d, f_{sw} further decrements by "$\Delta t_H/t_d$" steps. The event-time-driven technique is realized by edge detectors to detect $V_{det-1/2}$ edges direction, and digital counters to calculate Δt_H and Δt_L,

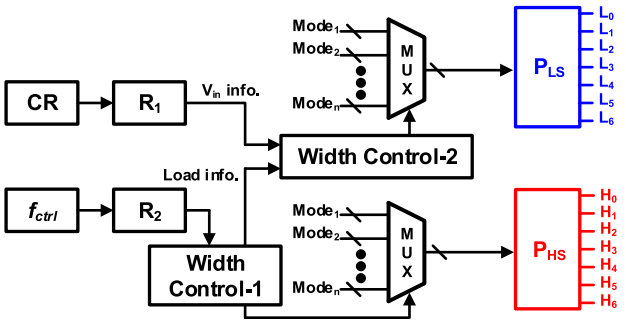

Fig. 13. Block diagram of the proposed SWM technique.

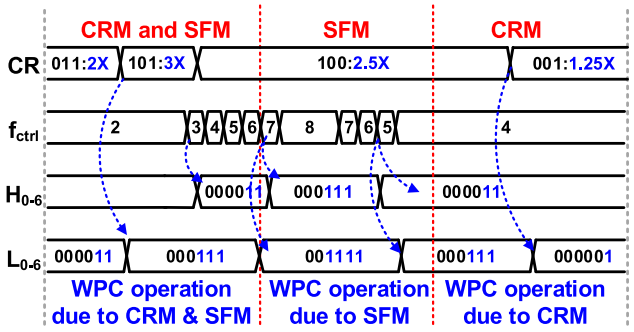

Fig. 14. Timing diagram of the proposed SWM technique.

as shown in Fig. 11. Finally, the SFM control block modulates the f_{sw} according to the sensed I_{load} condition, as described, by controlling a PROSC using an 8-bit f_{ctrl} digital signal.

3) SWM Control: The SWM control block optimizes the SP SCCP transistors size using L_{0-6} and H_{0-6} for P_{LS} and P_{HS}, respectively, (Fig. 11). Fig. 13 shows the SWM control block diagram. L_{0-6} is defined by two width controllers. They use the CR and f_{ctrl} stored in R_1 and R_2, respectively, to proportionally optimize P_{LS} size with I_{load} and V_{in} (i.e., V_{gs}) through a mode selector multiplexor and a 7-bit FFs. While H_{0-6} is only defined by one width controller, as shown in Fig. 11, since P_{HS} V_{gs} always equals V_{cp}. Likewise, the width controller-1 proportionally optimizes P_{HS} size with I_{load} through f_{ctrl} stored in R_2. The timing diagram shown in Fig. 14 explains the proposed SWM technique along with the SFM and CRM. L_{0-6} is updated with the CR and f_{ctrl} variations, while H_{0-6} is updated only with f_{ctrl}.

C. Programmable Voltage Detector (PVD)

The proportional modulation scheme of the SP SCCP transistors size with I_{load} varies according to V_{in} that defines the V_{gs} applied per transistor. Furthermore, to maintain regulation ($V_2 < V_{cp} < V_1$), and detect the load condition, V_{cp} must be continuously monitored. Conventionally, power-hungry blocks were used for this purpose such as voltage and current sensors [25], or a bandgap reference and a comparator [3], [4], increasing the power overhead. Thus, make it unsuitable for micro-EHS [8]. In the proposed 3-D MPPT, both the output and input voltages need to be detected for CRM, SFM, and SWM. The key building block in this

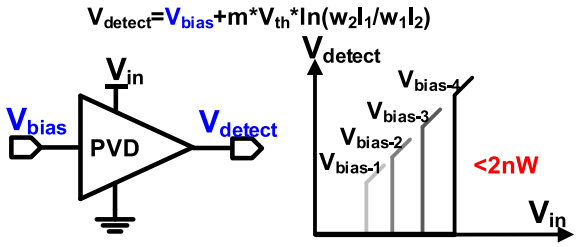

Fig. 15. Output illustration for the proposed PVD at different V_{bias}.

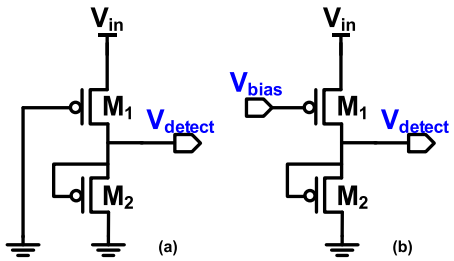

Fig. 16. Circuit schematic of the (a) conventional VD and (b) PVD proposed for the 3-D MPPT.

scheme is the ultra-low PVD (Fig. 8). Since the VDs load the input and output nodes, low power operation is required. To fulfill this requirement, a modified CMOS PVD version of the one presented in [26]–[28] is proposed with $\approx$ 2-nW power consumption to monitor V_{cp} voltage level and detect V_{in} range. The implemented PVD is a reference-less circuit with two inputs (V_{bias}, V_{in}) (Fig. 15), eliminating the need for bandgap circuit and power-hungry comparators or voltage and current sensors.

Fig. 16 shows the circuit schematics of the proposed PVD [Fig. 16(b)] and the one implemented in [28] [Fig. 16(a)]. The implemented VD schematic has been modified from the one proposed in [27] and [28], by connecting M_1 to V_{bias} for programmability. As described in [27], V_{detect} is defined as V_{in} when the VD output turns from 0 to 1, and that happens when I_{M1} equals I_{M2} as follows (assuming $V_{ds} > 100$ mV):

$$I_o\ w_1/l_1\ e^{\frac{V_{detect}-V_{bias}-V_{th1}}{mV_T}} = I_o\ w_2/l_2\ e^{\frac{-V_{th2}}{mV_T}} \tag{5}$$

where m is the subthreshold coefficient, V_T is the thermal voltage, and V_{th1} and V_{th2} are the V_{th} of and M_2, respectively.

Assuming the same m and V_{th} for M_1 and M_2 and by solving (5), V_{detect} can be given by

$$V_{detect} = V_{bias} + mV_T \ln \frac{w_2 l_1}{w_1 l_2}. \tag{6}$$

Thus, from (6), by varying V_{bias}, at a given w_2l_1/w_1l_2, the proposed PVD can detect five different ranges of V_{in}, as described in Fig. 12(a). Even though V_{detect} is proportional to temperature, it is not very critical for our application since the temperature variation is limited for PV and TEG EHS. However, the simulation results show a temperature-variation tolerance of 1 mV/°C in 0 °C–60 °C and a 4-mV variation across process variation.

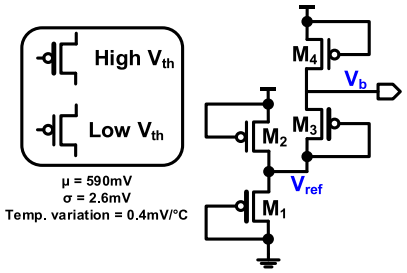

Fig. 17. Circuit schematic of the 4T voltage reference.

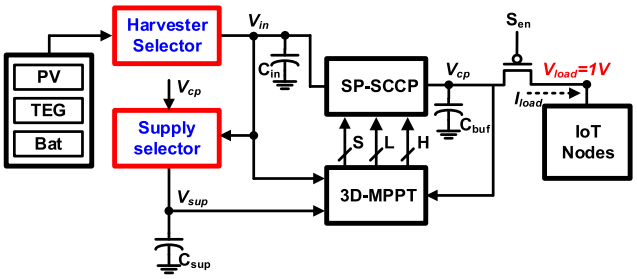

Fig. 18. Proposed MISO EHS architecture along with the harvester selector and the supply selector.

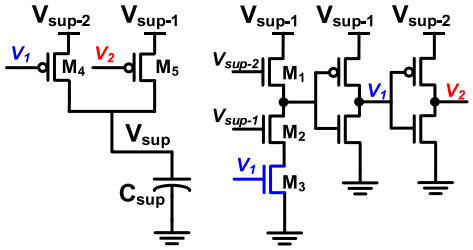

Fig. 19. Circuit schematic of the supply selector for cold startup.

D. 4T Bias Circuit

An ultra-low power 4T voltage reference followed by a diode-connected pMOS voltage divider affording multiple V_{bias} values is employed to bias PVD and PROSC for their programmability scheme (Fig. 8). The designed 4T reference circuit consumes 200 pW at 1 V as a voltage supply. With low threshold voltage and high threshold voltage pMOS devices, the process variation is about 0.5% and 2.3% for temperature variation (0 °C–60 °C). These numbers are acceptable for energy harvesting application, plus, the range of temperature is adequate for the applications of interest, as the temperature is not supposed to drift away from this range. Fig. 17 shows the schematic of the proposed 4T voltage reference along with the Monte Carlo data. In [28], a 2T voltage reference was used for another type of VD; however, as the reference voltage required is around 590 mV, 4T reference voltage circuit was used. The design equation that defines V_{ref} can be deduced by equating the subthreshold currents of M_1 and M_2 as follows:

$$I_o\ w_1/l_1\ e^{\frac{V_{\text{ref}}-V_{\text{th1}}}{m_1 V_T}} = I_o\ w_2/l_2\ e^{\frac{-V_{\text{th2}}}{m_2 V_T}}. \tag{7}$$

After rearranging (7), the following equation is obtained:

$$e^{\frac{V_{\text{ref}}-V_{\text{th1}}}{m_1 V_T}+\frac{V_{\text{th2}}}{m_2 V_T}} = \frac{w_2 l_1}{w_1 l_2}. \tag{8}$$

Here, m_1 and m_2 are the subthreshold slopes of M_1 and M_2, respectively. The temperature-dependent term V_T can be eliminated by equating the right-hand side of (8) to 1, in other words, by designing M_1 and M_2 so that $(w_2 l_1/w_1 l_2)$ equals 1, so that V_{ref} can be calculated as follows:

$$V_{\text{ref}} \approx V_{\text{th1}} - \frac{m_1}{m_2} V_{\text{th2}}. \tag{9}$$

Likewise, V_b, which is a boosted version of V_{ref} by adding M_3 and M_4, can be deduced using the same design equations of V_{ref}.

IV. Proposed EHS Operation Procedure

The EHS operation scheme includes three different modes, namely, the startup mode, the standby mode, and the normal mode. A cold startup technique is executed during the startup and standby modes, and employed without the need to any external battery or off-chip pre-charging mechanism, while the normal operation mode consists of the closed-loop operation of the proposed 3-D MPPT, and a proposed energy-aware technique. This section will discuss the proposed EHS operation procedure including the cold startup, the energy-aware operation, and the closed-loop operation.

A. Cold Startup Operation

Developing a cold startup technique is crucial for dc–dc converter within EHS [27], [29]. Fig. 18 shows the key building blocks for the cold startup mechanism, namely, the supply selector, and the VDs. The circuit schematic of the supply selector is shown in Fig. 19. V_{in} and V_{cp} are applied to $V_{\text{sup}-1}$ and $V_{\text{sup}-2}$, respectively, then the higher voltage is selected [$V_{\text{sup}} = \max(V_{\text{in}}, V_{\text{cp}})$] and used to power: 1) a differential ultra-low-power ring oscillator (RO) at startup and standby modes and 2) the 3-D MPPT circuit at normal operation mode. The RO used in startup and standby modes features high-frequency low power characteristics with temperature variation 8.9 KHz/°C. It provides at $V_{\text{in}-\text{min}}$ (350 mV) f_{sw} of 1.8 MHz with 22-nW power consumption, which makes it adequate solution for low-power EHS cold startup. The waveforms of the supply selector across different operation modes are shown in Fig. 20. Initially, the charges stored in C_{buff} equals "0," hence, the EHS operation sequence works as follows: first, during the startup mode, V_{cp} is less than V_{in}, so M_2 pulls V_1 up (V_1 = "V_{in}") and turns M_4 OFF, while it pulls V_2 down (V_2 = "0") and turns M_5 ON, hence, V_{sup} equals V_{in}. Second, once V_{cp} becomes greater than V_{in}, (standby mode) M_1 pulls V_1 down (V_1 = "0") turning M_4 ON and pulls V_2 up ($V_2 = V_{\text{cp}}$) turning M_5 OFF and allowing the startup circuit to be powered by V_{cp}. Finally, when the output VDs (Fig. 20) detect a high voltage at the output node ($V_{\text{cp}} \sim 1$ V), they trigger the DPU to connect the load circuit (S_{en} = "0") indicating the start of the normal operation mode.

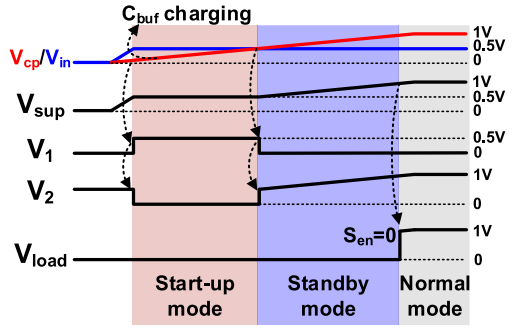

Fig. 20. Operation of the supply selector over different operation modes.

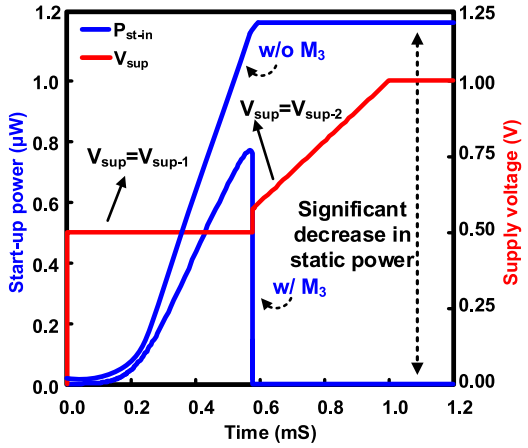

Fig. 21. Simulation results for the supply selector static power and output selected voltage.

The developed supply selector is modified from the conventional one presented in [30] by adding M_3 that significantly decreases the static on-current in M_1 and M_2 during the standby and normal operation modes. Fig. 21 shows the significant decrease in power consumption after adding M_3, beyond the startup operation mode.

B. Energy-Aware Operation

By connecting multiple dc energy scavenger to the EHS, a multiple-input-single-output (MISO) EHS can be obtained. As shown in Fig. 18, a PV cell, a TEG, and a backup battery are connected in parallel to a harvester selector block (HSB) that delivers the harvested energy from the PV cell or the TEG to the SP SCCP, or from the backup battery in case of low harvester energy. The HSB, shown in Fig. 22 is an energy-aware block that compares PV_{in} and TEG_{in} concurrently with $V_{\text{in-min}}$ (i.e., 350 mV) using a set of identical VD. Each VD triggers its outputs if and only if the harvester input exceeds the $V_{\text{in-min}}$. The results are fed to a logic circuit (Fig. 22) that adopts an energy-aware priority algorithm. Finally, S1, S2, and S3 control an IN–OUT selector to determine the energy harvester that will be connected to the SP SCCP. Following the timing diagram in Fig. 22, in case 1, PV_{in} is above $V_{\text{in-min}}$, indicating that it has excess energy, while TEG_{in} is less than $V_{\text{in-min}}$ which imply that it is low in energy.

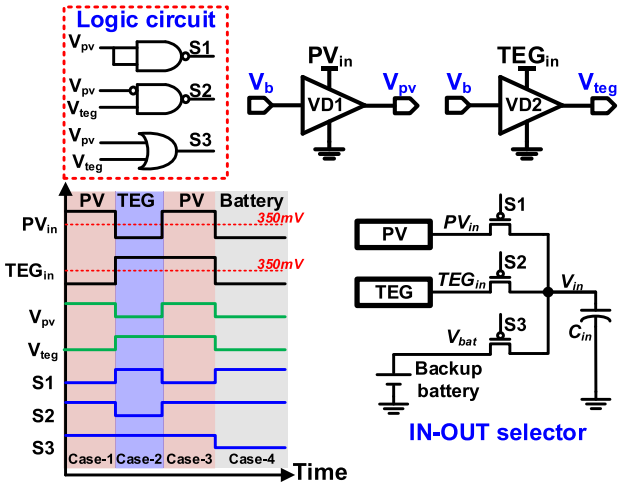

Fig. 22. Proposed HSB and operation timing diagram.

Thus, power is delivered from the PV to the EHS. Likewise, in case-2, TEG_{in} is selected to feed the SP SCCP, as it is above $V_{\text{in-min}}$. In another scenario, in case-3, PV_{in} and TEG_{in} are above $V_{\text{in-min}}$, which entails that both have excess energy. However, following the energy-aware priority algorithm of the logic circuit depicted in Fig. 22, PV_{in} is selected as an input for the SP SCCP. When both harvesters' inputs are below $V_{\text{in-min}}$, implying low harvesting energy, the backup battery is then used to feed the SP SCCP. Here, it is assumed that V_{bat} is always above V_{min}, for this reason, no VD is required to check V_{bat} dc level.

The proposed energy-aware algorithm is based on detecting the voltage levels of the two inputs (i.e., PV and TEG) as explained above. However, the harvester output voltage level (e.g., PV_{in}) may not be enough to categorize the amount of power a harvester can deliver since the amount of power depends on the harvester output resistance ($R_{\text{h-out}}$) as well. Although a low $R_{\text{h-out}}$is assumed so that the harvester output voltage can solely indicate the amount of input power, the proposed algorithm can be applied to high $R_{\text{h-out}}$, too. For example, high $R_{\text{h-out}}$ can make PV_{in} greater than V_{in} even if the PV is limited in power. This allows PV to be selected as the input and PV_{in} will go below $V_{\text{in-min}}$. In this case, the proposed algorithm will select the next harvester (i.e., TEG). Likewise, if TEG is limited in power, the backup battery will be used as the main input until PV and/or TEG have enough power. So, the proposed algorithm can use the harvester output voltage level as an indicator for the harvester power.

C. Closed-Loop Operation

The proposed EHS harvests solar and thermal energy to provide a regulated output voltage (1 V). It is composed of a forward path and a feedback path (Fig. 8). The forward path features a continuous V_{in} range detection, to set the proper SP SCCP conversion ratio. While the load condition is sensed using the feedback path, to establish the SP SCCP f_{sw}, W_{HS}, and W_{LS} accordingly.

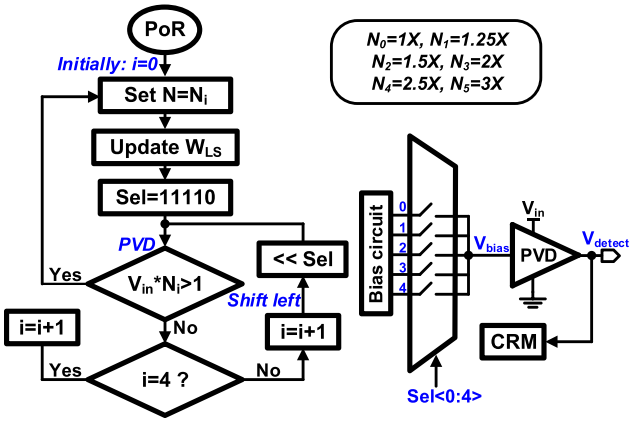

Fig. 23. Proposed 3-D MPPT forward path flowchart.

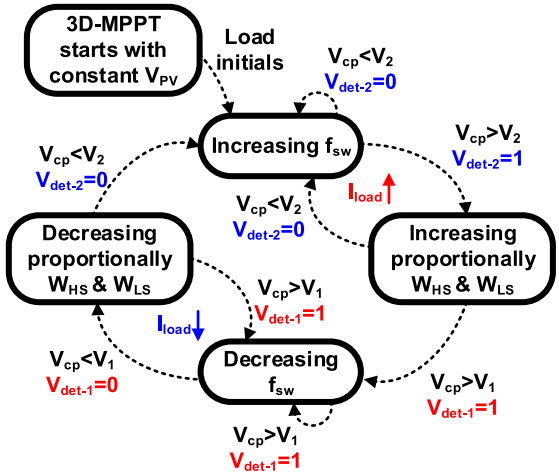

Fig. 24. Proposed 3-D MPPT feedback path state diagram.

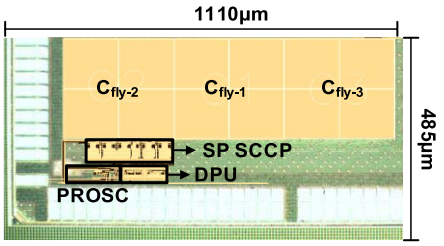

Fig. 25. Die photograph of the proposed EHS system.

1) Forward Path: The forward path architecture and flowchart are shown in Fig. 23. Initially, assuming normal operation mode, N is set to "1×." After the bias circuit stabilizes according to the active 4-bit "Sel" signal fed from the DPU, the PVD compares V_{in} with a certain boundary voltage equals "$V_{\text{cp}}/N_{\text{i}}$" set by the selected V_{bias} following (6). Following the flowchart depicted in Fig. 23, if the condition is true, the 3-D MPPT locks the SP SCCP conversion ratio "N" and set W_{LS} accordingly. However, if the condition is false, "i" is incremented by shifting the "Sel" signal one bit left, and the same condition is rechecked with the updated boundary voltage (V_{bias}) and so on. The loop repetition frequency is limited by the input energy harvester voltage variation.

2) Feedback Path: Within the feedback path, the proposed 3-D MPPT maintains regulation, determines the load state, and then updates the SP SCCP f_{sw}, W_{LS}, and W_{HS} accordingly. The output VDs set (Fig. 8) triggers their outputs, $V_{\text{det}-1}$ and $V_{\text{det}-2}$, (Fig. 12) when the V_{cp} cross the upper voltage boundary V_1 or the lower voltage boundary V_2, respectively, keeping V_{cp} within a narrow window [V_2, V_1]. The implemented TDC, comprising an edge detector and digital counter (Fig. 11), senses $V_{\text{det}-1/2}$ edges direction and measures their pulse periods. Fig. 24 shows the feedback path state diagram within the proposed 3-D MPPT. Initially, at a given V_{in}, if $V_{\text{cp}} < V_2$, which entails that the applied f_{sw} is not high enough for the instant I_{load} the 3-D MPPT DPU increments f_{sw} and proportionally increases W_{HS} and W_{LS}. Likewise, when an increase in V_{cp} is detected by the TDC, ($V_{\text{cp}} > V_1$), indicating an unnecessarily high f_{sw} for the current I_{load} (low load condition), the 3-D MPPT DPU decrements $f_{\text{sw}}$and decreases proportionally W_{HS} and W_{LS}. The proposed 3-D MPPT features a novel on-time tracking technique, which allows the MPP to be tracked without the need to retune or sweep the conversion ratio, and/or the switching frequency each MPPT cycle, as in [3]. On the contrary, f_{sw}, N, W_{HS}, and W_{LS} are decreased or increased concurrently by sensing the direction of I_{load} and V_{in}.

V. Measurement Results

The proposed 3-D MPPT along with the implemented SP SCCP IC chip was designed and fabricated in 65-nm CMOS process. The die microphotography of the fabricated chip is shown in Fig. 25. The integrated EHS including the 3-D MPPT and its auxiliary circuits occupies a silicon area of 0.538 mm^2. Three MIM on-chip capacitors are used for the SP SCCP flying capacitors implementation. The employed EHS harvests from 0.35 to 1 V and provides a regulated output voltage at 1 V with a <2-nW control circuit and an ultra-low power DPU.

The dynamic performance, within the feedback path, of the proposed 3-D MPPT is presented in Fig. 26. At a given V_{in}, the dynamic operation assumes three unique states. First, the reset state, where the tracking DPU receives a reset pulse to adjust the initial values of the f_{sw}, W_{LS}, and W_{HS} of the 3-D MPPT. During this state, the load is isolated from the EHS. Second, the constant load state, where I_{load} achieves its steady state. At light load (i.e., 500 nA), $V_{\text{cp}} > V_2$ and the resulted $V_{\text{det}-1}$ tends to decrease $f_{\text{sw}}$and the transistors width. Likewise, at heavy load condition (i.e., 0.3 mA), the output VDs transmit their $V_{\text{det}-1/2}$ pulses to the DPU to maintain regulation and to increase the applied f_{sw}, W_{LS}, and W_{HS}. The MPP, in both load conditions, is achieved when the SFM and SWM blocks, within the DPU, accommodate a proper switching frequency and transistors width with respect to the load condition. Finally, the transient state, when the load varies abruptly from 500 nA (light condition) to 0.3 mA (heavy condition), the DPU receives $V_{\text{det}-1/2}$ pulses to proportionally modulate the f_{sw} (SFM) and the SCCP transistors size (SWM) to track the MPP. Initially, $V_{\text{det}-2}$ triggers to increase f_{sw}, W_{LS}, and W_{HS} while $V_{\text{det}-1}$ turns "0," indicating an abrupt voltage drop due to a heavy load condition (Fig. 26).

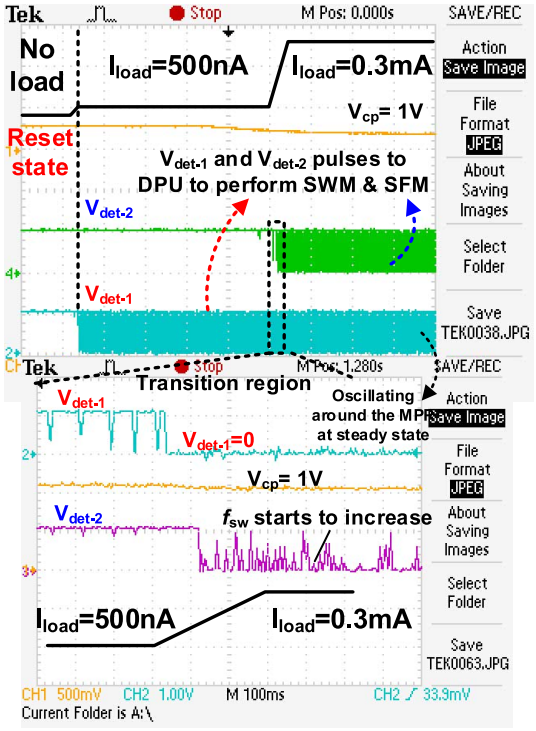

Fig. 26. Response of the proposed 3-D MPPT at a 0.3-mA load step.

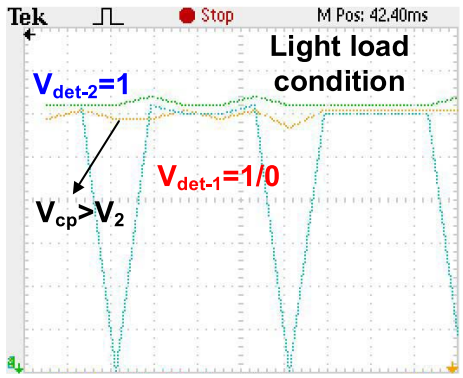

Fig. 27. Output VDs pulses at light load condition.

Fig. 27 shows the $V_{\text{det}-1/2}$ pulses at light load condition. Eventually, $V_{\text{det}-2}$ equals "1" as V_{cp} is greater than V_2, while $V_{\text{det}-1}$ pulses tend to maintain regulation and decreases the f_{sw} and transistors width to track the MPP. The measurements depicted in Fig. 28 shows the output regulation as V_{in} varies from 350 mV (low light irradiance) to 1 V (high light irradiance). As V_{in} varies across its range, the CRM control within the 3-D MPPT DPU alters W_{LS} in proportion to the applied V_{in} (V_{gs}) the achieve the MPP at a given output load.

The PE of the proposed 3-D MPPT using a PV-emulated power input circuit is recorded in Fig. 29 at different input voltages across the load range. The tested chip achieved a peak efficiency of 88% at 200 μA (heavy load), and a PE $>$60% at 100 nA (idle load condition). The efficiency results validate that the proposed 3-D MPPT algorithm as its adopted SWM technique shows the intended behavior not only at ultra-light loads but also at heavy load conditions. The proposed SWM technique improves the PE by at least 20% at light load

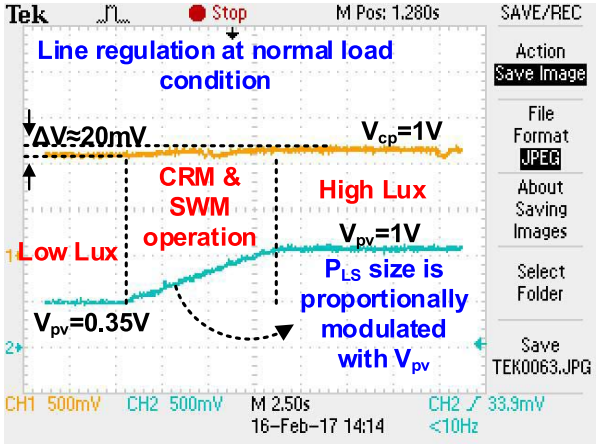

Fig. 28. Regulation performance of the proposed 3-D MPPT.

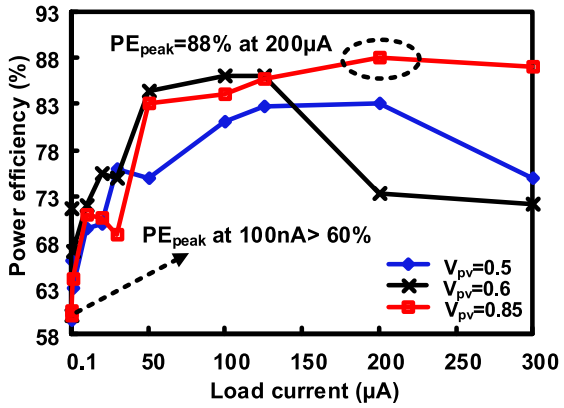

Fig. 29. PE at a different V_{pv} across the load range.

conditions ($<$1 μA), and by 10% at heavy load conditions ($>$ 100 μA) compared with the prior state-of-the-art works. This improvement is because of the proportional optimization of the SCCP transistor size with I_{load}, along with the SFM and CRM.

Table I shows the comparison with prior art EHS. The suggested 3-D MPPT improves the PE by at least 20% as compared with the MPPT design in [1] and [4]. Moreover, it can efficiently supply a $P_{\text{out}-\text{max}}$ of 0.3 mW using small silicon area, resulting in a higher cost efficiency, and power density compared with the prior art, make it an adequate solution for IoT smart nodes. Liu and Sánchez-Sinencio [4] uses a large capacitor bank for MPPT mechanism. Although it achieves a high efficiency of 86%, the PE degrades to less than 40% at light load conditions; moreover, the large die size makes it less cost effective and degrades its power density. The nested doubler charge pump presented in [3] increases the total conduction loss and the silicon area due to the considerable number of switches and the pumping capacitors. Hence, it is less cost effective and low in power density for IoT smart nodes. Our work proposed a novel tracking technique which IoT involves a reconfigurable feature regarding the switching frequency, the conversion ratio, and the charge pump transistor sizes, resulting in a 3-D MPPT. With total on-chip MIM flying capacitors of 240 pF, the integrated SP SCCP boosts V_{in} with six different conversion ratios to supply the IoT load

TABLE I
COMPARISON WITH PRIOR ARTS

Parameters	[1] ISSCC'16	[6] ISSCC'14	[11] ISSCC'14	[3] JSSC'16	[4] JSSC'15	[20] TCAS'11	This work
Technology	0.18µm	0.18µm	0.13µm	0.18µm	0.18µm	0.13µm	**65nm**
Fully integrated	Yes	Yes	No	Yes	Yes	Yes	**Yes**
Conversion ratios	Reconf.	Reconf.	Single	Reconf.	Single	Single	**Reconf.**
MPPT technique	SFM and CRM	SFM	No MPPT	SFM and CRM	CVM	No MPPT	**SFM, CRM and SWM**
Regulation	Yes	Yes	No	Yes	Yes	Yes	**Yes**
Output voltage	1.8V	2.2V-5.2V	0.619V	3.3V	3.3V	1.4V	**1V**
Input range	0.5V-1.8V	0.14V-0.5V	0.15V-0.45V	0.45-3V	1.1-1.5V	0.42-0.48V	**0.35V-1V**
Frequency range	NA	70Hz-19MHz	250KHz	20KHz-1MHz	250KHz	0.6MHz-1MHz	**19KHz-16MHz**
Output power range	<34.8µW	5nW-5µW	<60µW**	<50µW	<21µW	<10µW	**100nW-300µW**
Peak Efficiency	72%	50% @ 0.45V	35% @ 0.18V 72.5% @ 0.45V	89% @ 2.5V 85% @ 1.2V**	86.4%	65% @ 0.45V**	**83% @ 0.5V** **88% @ 0.85V**
Efficiency @ <1 µA	NA	40% @ 100nA**	<10% @ 1µA**	<50% @ 1µA**	<40% @ 1µA**	30% @ 1µA**	**60.5% @ 100nA**
Monolithic area	1.69 mm^2	0.86 mm^2	NA	4 mm^2	2.25 mm^2	0.42 mm^2	**0.54 mm^2**
Power density (µW/mm^2)	20.6	5.8	NA	12.5	9.3	23.8	**555.6**
Cold start-up	Yes	Yes	Yes	Yes	Yes	Yes	**Yes**

** extracted from the measurement results

with output power range from 100 nW to 0.3 mW, achieving the highest power density compared with the prior state-of-art designs. The implemented 3-D MPPT DPU complexity is reduced by using digital synthesis, minimizing the dynamic power consumption and making the proposed tracking technique scalable.

VI. CONCLUSION

The motivation behind this paper is to achieve a high PE at the light and idle modes, without sacrificing the high PE at heavy load conditions. To address this challenge, a novel tracking algorithm that eliminates gate-driver/conduction power loss tradeoff is proposed, showing a high PE across a wide load range compared with previous works. It successfully achieves a peak PE of 88% at 200 μA, and a PE of 60.5% at 100 nA. An energy-aware algorithm has been proposed to select the harvester and connect it to the EHS. The input harvesting range is extending from 0.35 to 1 V with a regulated output voltage at 1 V. The implemented MISO EHS is fully integrated with a cold startup without the need of external reference voltage or passive off-chip components, making it suitable for ultra-low-power applications within IoT smart nodes and wearable sensors.

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