A Highly Efficient Ultralow Photovoltaic Power Harvesting System With MPPT for Internet of Things Smart Nodes

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***Abstract*— Implementing a monolithic highly efficient ultralow photovoltaic (PV) power harvesting system is pivotal for smart nodes of Internet of things (IOT) networks. This paper proposes a fully integrated harvesting system in 0.18-μm CMOS technology. Utilizing a small commercial solar cell of 2.5 cm^2, the proposed system can provide 0–29 μW of power, which is much higher than the commonly used passive radio-frequency identification devices in IOT application. The hill-climbing maximum power point tracking algorithm is developed in an energy-efficient manner to tune the input impedance of the system and guarantee adaptive maximum power transfer under wide illumination conditions. The detailed impedance tuning approach is implemented with a capacitor value modulation to eliminate the quiescent power consumption as well as to achieve a higher efficiency than the traditional pulse-frequency modulation scheme. A supercapacitor is utilized for buffering, energy storing, and filtering purposes, which enables more functions of the IOT smart nodes such as active sensing and system-on-chip (SOC) signal processing. The output voltage ranges between 3.0 and 3.5 V for different device loads, such as sensors, SOC, or wireless transceivers. The measured results confirm that this PV harvesting system achieves both ultralow operation capability under 20 μW and a self-sustaining efficiency of 89%.**

***Index Terms*— Capacitor value modulation, energy harvesting, Internet of things (IOT), maximum power point tracking (MPPT), solar cell.**

I. Introduction

With recent developments in the microelectromechanical system sensors and scaling down of the silicon fabrication technology, the Internet of things (IOT) has been proposed to uniquely identify objects and their virtual representations in an Internet-like structure [1]. Under such configuration, every object within the network can be tagged, analyzed, and managed to compose the event-driven mechanism of an IOT system [2]. As a leading topology and specific implementation of IOT, a wireless sensor network (WSN) has been created to monitor, communicate, and process environmental information [3], [4]. In the WSN, the distributed sensors, also called smart nodes, should be integrated with SOC and wireless transceivers. The main practical challenge is how to power multiple electronic devices. Based on the self-sustaining operation scenario, the smart node is attached to objects without a power or signal wire connection. Since the occupied area of the harvesting system should also be minimized for monolithic integration, the available photovoltaic (PV) power is stringently limited, mandating the harvesting system to be highly energy efficient. Another design challenge is the fact that the PV energy resource changes its power density depending on different environmental variables such as illumination intensity and temperature [5]. Thus, it requires the harvesting system to be adaptive to those environmental variations to achieve maximum power transfer.

Currently, radio-frequency (RF) electromagnetic waves are utilized to power RF identification devices (RFIDs) [6]–[8]. However, RFID acts as a passive transponder to the WSN only when RF power resides within a certain frequency range. Thus, the operation of a distributed smart node is not event driven but scanned by an RF reader, resulting in passively monitoring. Trying to solve this issue, researchers have proposed a battery-assisted passive RFID, which can actively transmit its sensed information using a small rechargeable on-board battery [9]. However, the reliability, size, and lifespan of the on-board batteries are not satisfying and limit the development of the IOT [2].

In this paper, a practical approach of PV energy harvesting is proposed as a power supply for the IOT smart nodes. The power supply allows its loads such as sensors or SOC to actively and periodically process and transmit data, rather than be invoked by an RF reader. There are several key features of the proposed harvesting system. First, a switched capacitor dc–dc converter is chosen to eliminate the need for an off-chip inductor, making it a monolithic solution suitable for the fully integrated IOT smart nodes. Second, maximum power point tracking (MPPT) technique is applied to adapt illumination and temperature variations. The MPPT module provides an optimal impedance tuning between PV cells and the harvesting system. Thus, it enables maximum input power transfer under different illuminating conditions. From the energy dissipation point of view, the system controller is realized in mixed-signal circuits, which consume less power than conventional MPPT modules due to the ultralow PV power budget [10]. Thus, the harvesting efficiency is improved by maximizing the input PV power and minimizing the quiescent energy of control circuits. Third, instead of commonly used frequency modulation scheme [10],

Manuscript received April 2, 2014; revised October 17, 2014; accepted December 14, 2014. Date of publication February 26, 2015; date of current version November 20, 2015.

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Digital Object Identifier 10.1109/TVLSI.2014.2387167

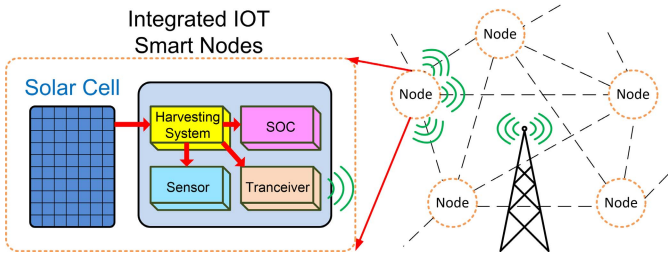


Fig. 1. Electromechanical model of the piezoelectric transducer at resonance.

the specific impedance tuning method in this particular design uses a capacitor value modulation approach with a fixed switching frequency. Although reported in [11] for load regulation, this paper first proposes the capacitor value modulation for impedance tuning. Thus, the harvesting system achieves less quiescent power consumption and predictable electromagnetic interference (EMI) [12]. Finally, the harvesting system is proposed to be self-sustaining, using a startup circuit and an auxiliary charge pump supplied by the input PV energy, and generate all the switching signals and voltage references, eliminating the needs of external clocks and biases. At the output of the system, a supercapacitor technique is utilized to store and deliver energy to the loads in a dark environment without available PV power. This supercapacitor could be also replaced by a rechargeable battery, such as Li-ion battery.

II. Adaptive PV Energy Harvesting System

A. Integrated IOT Smart Nodes

The IOT can be implemented by tagging objects, as shown in Fig. 1. The main difference from the conventional passive tag is that an IOT smart node includes a small-size energy harvester, supercapacitor/battery, SOC, wireless transceiver, and sensor. The indoor light is widely applied in living environments and has a higher power density when compared with the RF electromagnetic wave emitted by the RFID reader [8]. The small solar cell embedded in the smart node can be a more flexible, robust, and efficient power supply. Thus, the distributed nodes of WSN can actively sense and exchange information with each other by low-power communication technologies such as ZigBee or Bluetooth. The WSN can be widely applied in various applications, such as smart electrical grids, logistic flows, military or security wireless guards, and natural disaster sensor networks for forest fires, tsunamis, or earthquakes [3].

B. Architecture of the Proposed Energy Harvesting System

The proposed structure of the adaptive harvesting system is shown in Fig. 2, where FSM is a finite-state machine. Note that the switching-mode dc–dc power converter using an inductor or a transformer, such as a boost converter, features high transferring power density and efficiency [14], [15]. However, the high-quality on-chip inductors are not widely available for the CMOS technology. Therefore, to achieve monolithic integration, a charge pump, shown in Fig. 2, is chosen for its compact on-chip capacitor. As a direct interface to the solar cell, the charge pump boosts the input PV voltage to the required level and delivers the PV energy to the supercapacitor and loads. A current sensor, MPPT module, and digital controller compose the feedback path. To achieve smart control of IOT networks, an I/O communication interface is designed to exchange information with external WSNs.

The power conversion efficiency (PCE) is the most crucial figure of merit of the design of harvesting system topologies. With a PV cell size of 10 mm $\times$ 25 mm and 200 lux illumination, the available power is below 11 μW, which is a stringent power budget on the harvesting method. Therefore, the analog control schemes using several operational amplifiers are not feasible due to the quiescent power consumption [13].

Furthermore, the control strategy should extract as much energy as possible from the PV energy source. However, the PV maximum power point (MPP) or equivalent impedance is not constant but shifted with the environmental parameters such as illumination intensity and temperature. Thus, a dynamic MPPT algorithm is a must to track the output impedance of solar cell Z_{solar} and achieve a maximum power transfer. In general, the MPP decreases with lower light intensity and higher temperature. Based on this topology, the straightforward hill-climbing algorithm of MPPT is chosen to minimize the hardware complexity and power consumption [16]. To dynamically track the MPP in Fig. 2, information of the output power delivered from the charge pump to the loads needs to be extracted. Since output power P_{out} is filtered by the supercapacitor to maintain a constant voltage, output current I_{out} is proportional to P_{out} and can be monitored by a current sensor. Due to the ultralow PV power, the entire load current is used for sensing. Therefore, to minimize its power consumption, the current sensor is only powered ON during the short MPPT procedure. During the other time, it is shut down and bypasses the harvested power to the load. The detailed MPPT mechanism will be discussed in Section II-C.

Last but not least, the specific parameters that allow MPPT impedance tuning are also critical to the structure of the harvesting system. Ideally, the input impedance of a charge pump Z_{cp} is provided by the product of switching frequency f_s and capacitor values C_u. Conventional solar energy harvesters employ various kinds of frequency modulation by tuning the switching frequency f_s or duty ratio D [10], [14], [17]. However, the power consumption of the frequency modulator is not negligible and strongly affects the overall energy harvesting efficiency. Thus, in the feedback path of Fig. 2, a self-biased switch-type current sensor with an energy-efficient capacitor value modulation scheme is proposed instead of the conventional pulse-width modulation (PWM) and pulse-frequency modulation (PFM) schemes. As a result, it avoids quiescent power consumption.

C. Energy-Efficient MPPT With the Hill-Climbing Algorithm

To realize the hill-climbing algorithm with a limited power budget, an energy-efficient MPPT module is proposed in Fig. 2. It compresses logic steps and applies minimum devices, including two sample-and-hold (S/H) channels, comparator, digital controller, and modulated capacitor bank. Their

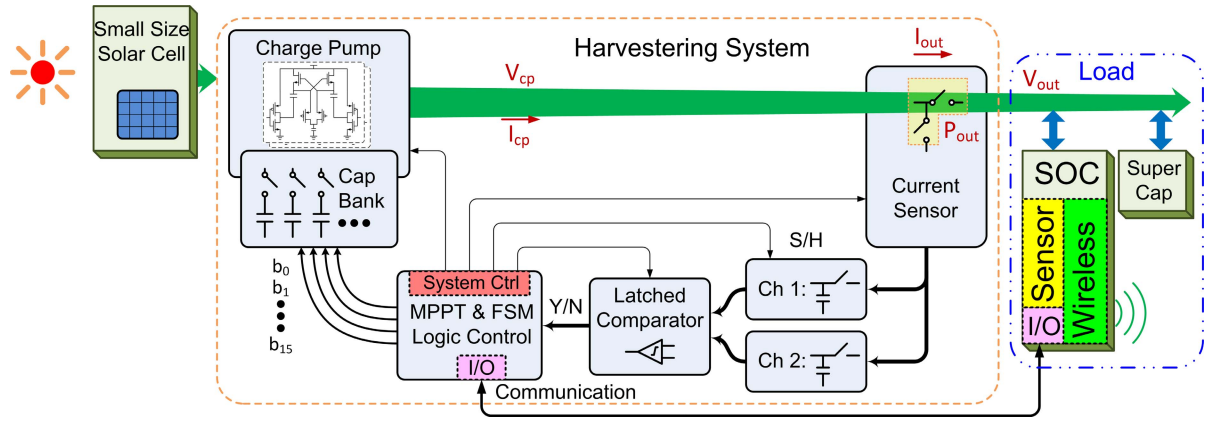


Fig. 2. Block diagram of the proposed energy harvester with the MPPT technique.

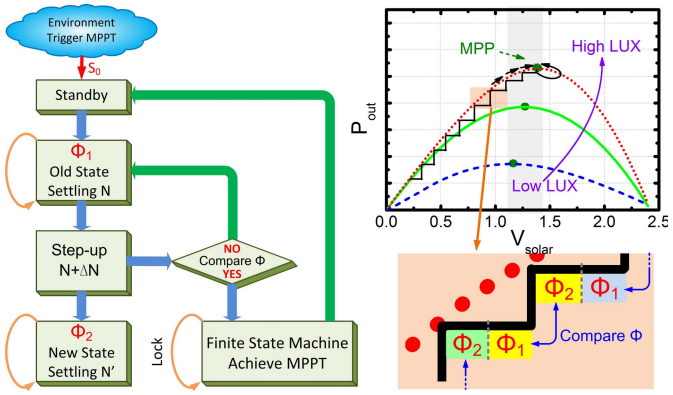


Fig. 3. Flow chart of adaptive MPPT and MPP moving curve during tracking procedure.

functional flow chart and conceptual hill-climbing procedure are shown in Fig. 3. An enable signal S_0 triggers the MPPT procedure, which is provided by a periodic timer or an environmental sensor of the WSN. As shown in Fig. 3, the sensing phases are divided into two, Φ_1 and Φ_2, by tracking the power information of old and new slots. Each phase requires several clock cycles to reach a steady state. After that, Φ_1 and Φ_2 are compared through the low-power comparator. The comparator latches and indicates whether the new tentative tuning step is improving or not. A digital controller is used to control the entire system, as well as to communicate with other IOT smart nodes.

D. Capacitor Value Modulation

A voltage doubler shown in Fig. 4(a) features minimum components for required conversion ratio (CR). With complementary switching clocks V_{ck1} and V_{ck2}, the converter charges the solar cell voltage V_{solar} across C_u and then levels up its negative plate by the same potential. In a steady state, the resulting output voltage V_{cpo} is twice of the input voltage V_{solar}. However, only one stage with twice 2× CR is not enough between the photovoltage 1-1.5 V and the 3 V supply, which is typically required by the smart node loads. Thus, as shown in Fig. 4(b), two voltage doublers are nested and the second doubler has one modified input from V_{solar}, resulting in a CR of 3. The steady-state

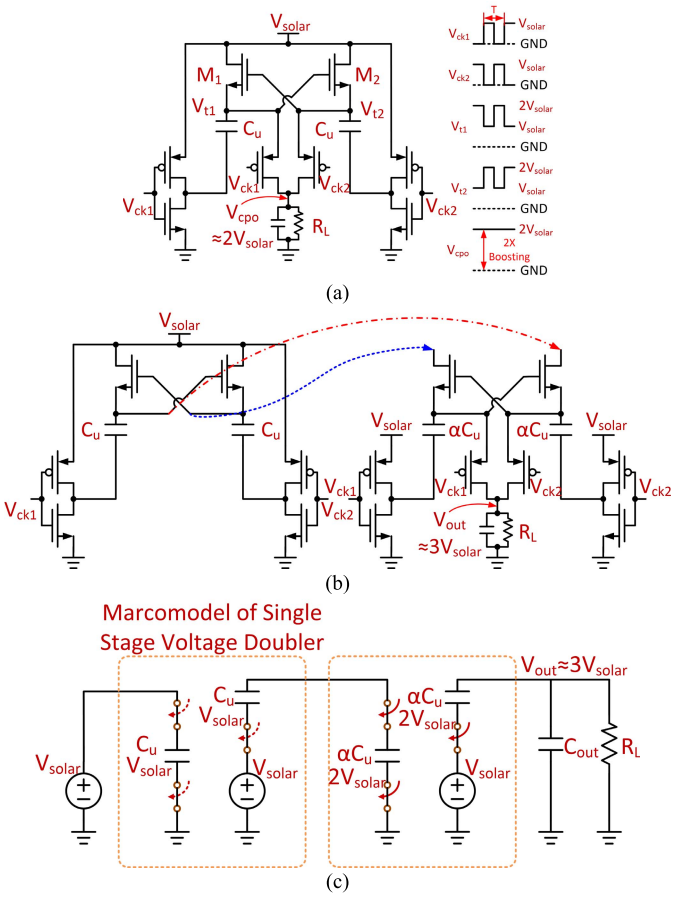


Fig. 4. (a) Principle of the voltage doubler. (b) Nested voltage tripler built with two voltage doublers. (c) Macromodel of the voltage tripler.

macromodel can be simplified by neglecting parasitics, as shown in Fig. 4(c). α is the capacitor ratio factor between the second and the first stage. Applying the principle of charge conservation

$$[2V_{\text{solar}} - (V_{\text{out}} - V_{\text{solar}})] \times \alpha C_u = \frac{1}{2} \times \frac{T \times V_{\text{out}}}{R_L} \quad (1)$$

where the T and R_L stands for switching clock period and equivalent load resistance of SOC, respectively. Due to the buffer and filter function of the supercapacitor, the load voltage V_{out} is dc. Thus, V_{solar} can be expressed as a function of

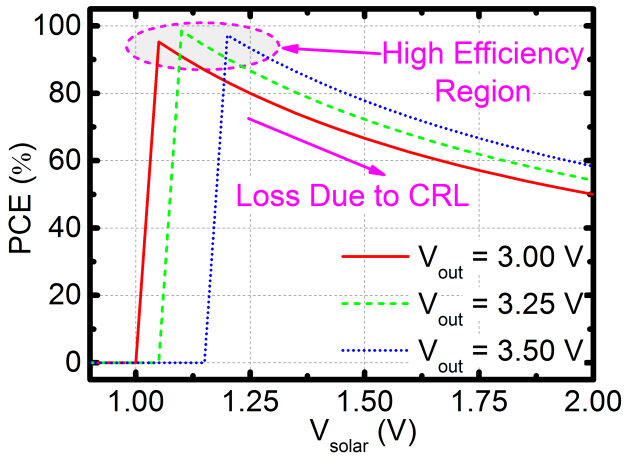


Fig. 5. PCE versus V_{solar} with 3–3.5 V V_{out}.

multiple variables, yielding

$$V_{\text{solar}} = \left(\frac{1}{2} \times \frac{T}{R_L} \times \frac{1}{\alpha C_u} + 1\right) \times \frac{1}{3} \times V_{\text{out}} \xrightarrow{\text{Match}} V_{\text{MPP}}. \quad (2)$$

Without any loading effect, the theoretical ratio between the input and output voltages is 1:3. With variable loads, the input voltage V_{solar} can be tuned by two parameters to match the MPP V_{MPP} of solar cell: 1) switching frequency $f_s = 1/T$ and 2) switching power capacitor C_u. Although first proposed in charge pump power converter, the capacitor value modulation was used for load regulation [11]. In this energy harvesting system of IOT smart nodes, we propose the variable C_u to do the impedance tuning for MPPT. The generation of variable f_s usually needs complex auxiliary circuits and consumes a significant amount of power, thus affecting the efficiency of the harvester system [10]. Therefore, the approach of the power capacitor tuning with fixed f_s is chosen for three major benefits.

1) The power capacitor can be digitized into a bank of multiple value capacitors. The passive components do not consume quiescent power and its digital controller needs little dynamic power. Such intrinsic characteristics guarantee the high efficiency of the converter.
2) The constant switching frequency f_s gives predictable noise spectrum and alleviates the EMI problems on the sensor loads.
3) The increase of chip area due to the programmable capacitor is minimal, because the low harvested energy only requires small-size on-chip capacitors, taking 1.03 mm^2 active area with IBM 0.18-μm process. It can also be scaled down with other CMOS technologies.

E. Efficiency Limit by the Charge Redistribution Loss

The switched capacitor topology causes an inevitable charge redistribution loss (CRL) [18]. The affected PCE of the charge pump can be estimated as

$$\text{PCE} = \frac{V_{\text{out}}}{V_{\text{solar}} \times \text{CR}} \times 100\% \quad (3)$$

where CR equals to three for this specific topology. The PCE with various input and output voltages is shown in Fig. 5.

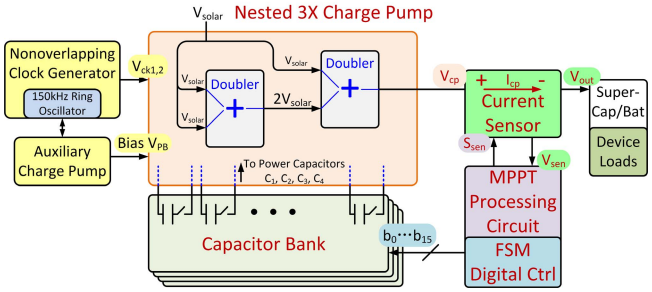


Fig. 6. Conceptual block diagram of the proposed energy harvesting system.

The result indicates that the ratio between V_{out} and V_{solar} should not deviate much from CR = 3 to avoid the CRL affecting the PCE. Because V_{out} is pinned to 3–3.5 V by the output supercapacitor or battery, the MPPT matched V_{solar} should be in the vicinity of 1–1.5 V to achieve a high PCE with minimum CRL.

III. System Block Implementation

The proposed energy harvesting system shown in Fig. 2 is implemented with conceptual blocks as Fig. 6 and will be discussed block by block in the following.

A. Nested Voltage Tripler

The Dickson charge pump is widely used in solar energy harvesting. However, it provides a low-voltage CR. Therefore, a CR-improved structure of the nested voltage tripler is chosen, as shown in Fig. 7(a). The first stage provides two times voltage boosting, and the nested second stage provides 1.5 times voltage boosting, resulting in an overall CR of three. In Fig. 4(a), the switch transistors M_1 and M_2 are cross connected and self-switched. However, such architecture limits the turn-ON voltage of nMOS transistors to less than V_{solar}, which ranges from 1 to 1.5 V. The low turn-ON voltage drastically increases the conduction resistance and degrades the boosting efficiency. To generate enough gate overdrive, we propose to break the cross-connected gate and drive them with a higher voltage separately. Moreover, the direct driving scheme does not have several coupled parasitic issues and the need for damping branch compared with the self-switching scheme [19].

The impedance of the proposed charge pump can be extracted from the model in Fig. 4(c) as

$$Z_{\text{cp}} = \frac{V_{\text{solar}}}{I_{\text{in}}} = \frac{1}{2 f_s C_u} \frac{1+\alpha}{\left(3 - \frac{V_{\text{out}}}{V_{\text{solar}}}\right)\alpha} \quad (4)$$

which verifies that the impedance of the charge pump is inversely proportional to f_s and C_u. Thus, Z_{cp} and Z_{solar} under different light intensities are plotted in Fig. 7(b) with f_s = 150 kHz, $V_{\text{out}}/V_{\text{solar}}$ = 2.6, and α = 4. With programmable C_u between 18 and 138 pF, the proposed charge pump successfully matches the impedance of PV cell under 150–800 lux.

In Fig. 7(c), an auxiliary charge pump is used as a level shifter to generate 3 × V_{solar} switching signal for the voltage tripler. As a result, the nMOS transistors $MN_{1,2}$ have a gate

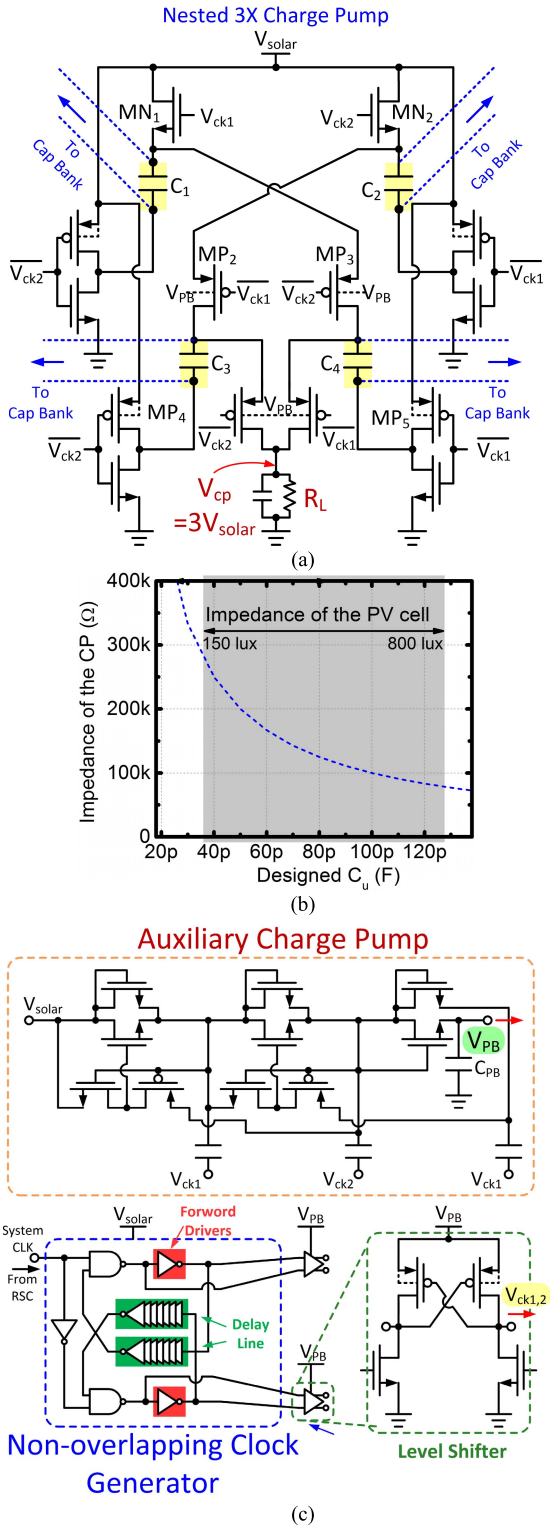


Fig. 7. (a) Detailed structure of the nested voltage tripler. (b) Impedance of the charge pump Z_{cp} with designed C_u values versus impedance of PV cell Z_{solar} under different light intensities. (c) Auxiliary charge pump, nonoverlapping clock generator, and level shifter.

drive voltage of $2 \times V_{solar}$ during the turn-ON period. In addition, the auxiliary circuit, in Fig. 7(c), will provide $3 \times V_{solar}$ to all control circuits as a power supply and body bias. Due to the minimal gate capacitance of switches, the auxiliary charge pump has only 1/8 the size of the main voltage tripler to minimize the parasitics. All the switching clocks are provided by a nonoverlapping signal generator shown in Fig. 7(c), which eliminates the shoot-through current and improves the converter efficiency. Different from the conventional NAND based nonoverlapping clock generator, a delay line is placed in the feedback path. Therefore, the forward drivers are designed to maximize their fanout capability and minimize their power consumption. The nonoverlapping time is tuned by the delay line independently.

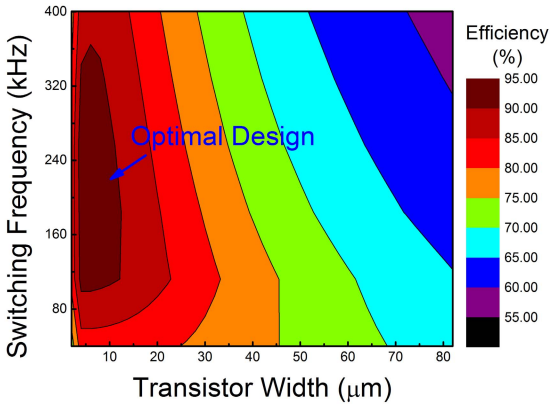


Fig. 8. Efficiency tradeoff between the power transistor gate width W_u and switching frequency f_s.

To realize the self-sustaining feature for the adaptive harvesting system, the entire control unit is powered by the circuits in Fig. 7(c). Thus, they also function as a startup module to help the system wake up. Once the solar cell is connected to the harvester, the ring oscillator begins to generate a switching clock. The auxiliary charge pump, in Fig. 7(c), will quickly charge the self-sustaining capacitor C_{PB} to V_{PB} as a startup.

A detailed optimal design strategy can be derived for maximizing the efficiency. Referring to the steady-state model, the total power loss of the power converter is determined by

$$P_{loss} = P_{cond} + P_{cap} + P_{CRL} \tag{5}$$

where P_{cond}, P_{cap}, and P_{CRL} stand for the conduction loss, the parasitic capacitor dynamic loss, and the CRL, respectively. According to these boundaries, the optimized unit gate width can be calculated for the minimum total power loss. The optimal device dimension W_u is based on the switching frequency f_s and fabrication technology. A detailed efficiency tradeoff between f_s and W_u is simulated in Fig. 8. Because the low harvested power only needs small active devices, the optimal f_s has a wide range due to their minimal parasitics. Referring to (5), the conduction loss of power transistors dominates. Thus, in the vicinity of maximum conversion efficiency, we choose f_s of 150 kHz as the design specification.

B. MPPT Mechanism and FSM Design

In Fig. 6, the MPPT mechanism is implemented by five synchronous D-flip-flops and periphery logic gates. The clock timing diagram is shown in Fig. 9, and its simulated operation is shown in Fig. 10. One cycle of the MPPT procedure is

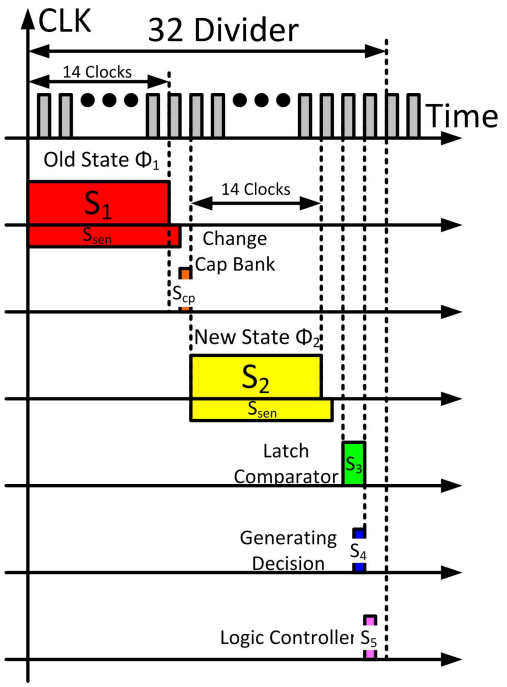


Fig. 9. Designed time diagram of the MPPT controller.

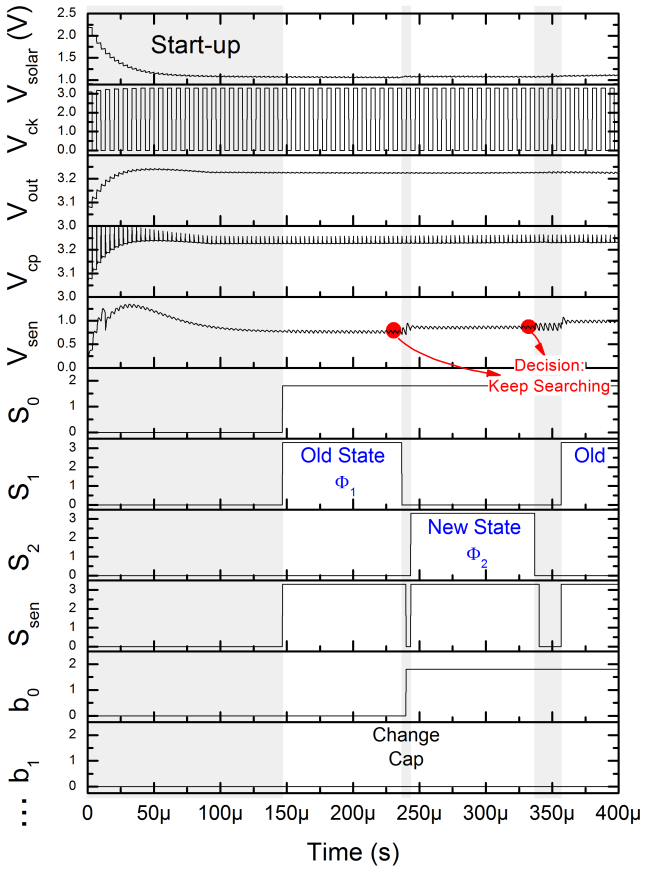


Fig. 10. Simulated waveforms of the FSM for the MPPT procedure.

executed during 32 clock periods. At the beginning of MPPT, all the capacitors in the bank are connected. The solar cell has the heaviest load, and the FSM will disconnect those capacitors by the algorithm. After a number N is counted into the programmable capacitor bank, the harvesting system uses 14 cycles to settle down in this condition. At the end of the settling period, a power sensor captures the stabilized output current value, which is proportional to the harvested power P_n. An S/H circuit accurately samples P_n from power sensor during this period and holds the value by the falling edge of S_1. Half a clock delay is given as the margin between sampling signal S_1 and sensing signal $S_{\rm SEN}$. Once the value is held, the capacitor bank is configured to a new N' in the later half clock. Simultaneously, a reset-and-sample command S_2 is sent to another identical S/H circuit for another 14 clocks to follow the information of the new output power P_{n+1}. When Φ_2 for N' capacitor bank is finished, signal S_3 outputs the harvested power information for two clock periods, which means comparison ready. With signal S_4, the logic decision is generated through a latch. Finally, triggered by S_5, the FSM digital controller executes digital processing based on the result. As the signal flow chart shown in Fig. 3, if P_{n+1} of the new state is larger than P_n of the old state, the FSM keeps searching the optimal point. Otherwise, the peak power has passed and the FSM goes back to state P_n so that the maximum power transfer is realized.

C. Current Sensing Technique With Ultralow Power Consumption

As shown in Fig. 6, a current sensor instead of power sensor is used to monitor the harvested energy. However, most conventional current sensors are not specifically designed for ultralow currents. By utilizing current mirrors and operational amplifiers, they cannot guarantee accurate current distribution against process variation and enough sensing sensitivity for this ultralow PV energy scenario [10].

The low currents and high gain factor are the main challenges. The output current of the system is around several microamperes, which prevents the system to perform any current division or engage large bias currents. Therefore, we propose a power-efficient current sensor, as shown in Fig. 11(a), where $V_{\rm cp}$ is the output voltage shown in Fig. 5. To minimize the power consumption, sensing state $S_{\rm sen}$ and standby state $\overline{S_{\rm sen}}$ are implemented by $\rm SW_{C1}$ and $\rm SW_{C2}$. During the sensing phase with $\rm SW_{C2}$ turned ON, all the current from the voltage tripler goes into the right branch, while the reference branch is controlled by the supercapacitor voltage $V_{\rm out}$. To make sure equal voltage potential between $V_{\rm out}$ and $V_{\rm cp}$ to be held, the self-biased current amplifier uses positive feedback through $M_{\rm CP1}$, $M_{\rm CP2}$, $M_{\rm CN1}$, and $M_{\rm CN2}$ to boost its loop gain. The closed-loop transfer function from the output current of charge pump to the sensed voltage can be derived as

$$\frac{V_{\rm sen}}{I_{\rm cp}} = \frac{R_{\rm SEN}}{1+\frac{1}{g_{\rm MCP3}}\cdot T_{\rm FB}} \tag{6}$$

where $T_{\rm FB}$ represents the open-loop transconductance through the blue dashed path as

$$T_{\rm FB} = \frac{i_2}{V_{\rm cp}-V_Y} = \frac{1}{\frac{1}{g_{\rm MCN2}\times(-g_{\rm MCP1})\times Z_{\rm CN1}} + Z_{\rm CP2} - \frac{1}{g_{\rm MCN2}}}. \tag{7}$$

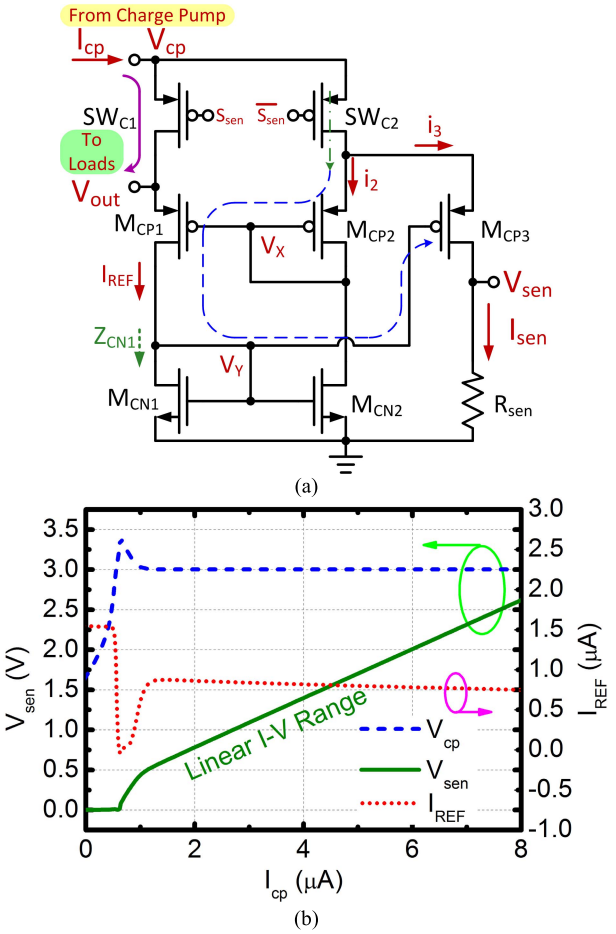


Fig. 11. (a) Proposed structure of the current sensor. (b) Characteristics of sensing voltage V_{sen} and reference current I_{REF} versus throughput current I_{cp}.

With a symmetrical design, we have $Z_{N1} \approx 1/g_{\text{MCN1}}$ and $Z_{P2} \approx 1/g_{\text{MCP2}}$ at low frequencies. The above transfer function can be simplified as

$$\frac{V_{\text{sen}}}{I_{\text{cp}}} = \frac{R_{\text{sen}}}{1 - \frac{g_{\text{MCN2}}}{g_{\text{MCP3}}}}. \tag{8}$$

From the denominator, both positive and negative feedback through g_{MCN2} and g_{MCP3} affect the overall current sensing gain. In this design, the width and transconductance of M_{CP3} are made much larger than M_{CN2}. Therefore, the negative feedback dominates to ensure the stability and eliminate potential startup difficulty. The transfer characteristic is shown in Fig. 11(b). Once the small self-biased current is exceeded, the two node voltages V_{cp} and V_{out} are forced to be equal, and the current information I_{cp} is amplified and converted monotonically into V_{sen}.

D. MPPT Processing Circuit

As shown in Fig. 6, when the current sensor starts evaluating the output power, the S/H MPPT module is simultaneously triggered to record and compare the power information. As shown in Fig. 12, the detailed MPPT processing circuit consists of two identical S/H channels, a comparator, an FSM, and a binary-to-thermometer decoder.

The two identical channels, in Fig. 12, are controlled by complementary phase clocks S_1 and S_2. Defined by the digital controller, phase S_1 is set to capture the power information of the old state and phase S_2 for that of the new state. Finally, the two states relating to different charge pump capacitor values are stored and aligned for latch comparison. During the current sensing period S_{SEN}, the voltage tripler is disconnected from the supercapacitor load to the current sensor, which induces noticeable voltage ripples. However, as shown in Fig. 12, the combination of the sampling capacitor $C_{\text{S/H}}$ and the large resistor R_{SEN} acts as a low-pass RC filter, thus extracting the dc value correctly. Due to the ultralow power budget and one-time comparison requirement, we choose the latched comparator. A positive feedback of the latched comparator is used to boost the regeneration gain. The transistor size is minimized for low energy consumption. The proposed capacitor value modulation scheme replaces analog modules with digital modules, such as the comparator, the FSM, and the decoder. The digital modules operate in low speed under low power supply, resulting in negligible power consumption.

E. Digital Programmable Capacitor Bank of Capacitor Value Modulation

The digital programmable capacitor bank shown in Fig. 6 is implemented in this section. With the manipulation from the MPPT module, the capacitor value of the bank, also as the input impedance of the charge pump, is modulated to track the MPP of a solar cell. As shown in Fig. 12, the capacitor bank consists of a static part C_s and a programmed part C_P. The C_s delivers the minimum usable power. The C_P is split into coarse and fine impedance tunings. The coarse tuning uses 15 identical capacitors programmed by a 4-bit FSM controller. Instead of binary code, thermometer code is used for smoother transition during most significant bit changing. The fine-tuning resolution has 1/2 the value of the standard capacitor C_P and controlled by 1-bit additional binary code. During the MPPT procedure, the 4-bit coarse capacitor bank keeps being programmed. Once the maximum power transfer range is locked, the fine tuning is executed in the subloop to improve the tracking accuracy.

IV. Experimental Results

The adaptive PV harvester system is designed and fabricated in the standard 0.18-μm CMOS technology. The die photo of the fabricated chip is shown in Fig. 13(a). The entire energy harvesting system occupies a silicon area of 1.5 mm $\times$ 1.5 mm. Dual-layer metal–insulator–metal on-chip capacitors are used for the monolithic integration of the capacitor bank. The testing setup is demonstrated in Fig. 13(b). The indoor illumination environment was calibrated by a light meter.

The transient measurements were carried out to verify the correct behavior of the MPPT module. To emulate mild indoor illumination, a light intensity of 400 lux was given. The light acceptor was a small commercially available solar cell featuring 10 $\times$ 25 mm^2 in size. The load was characterized

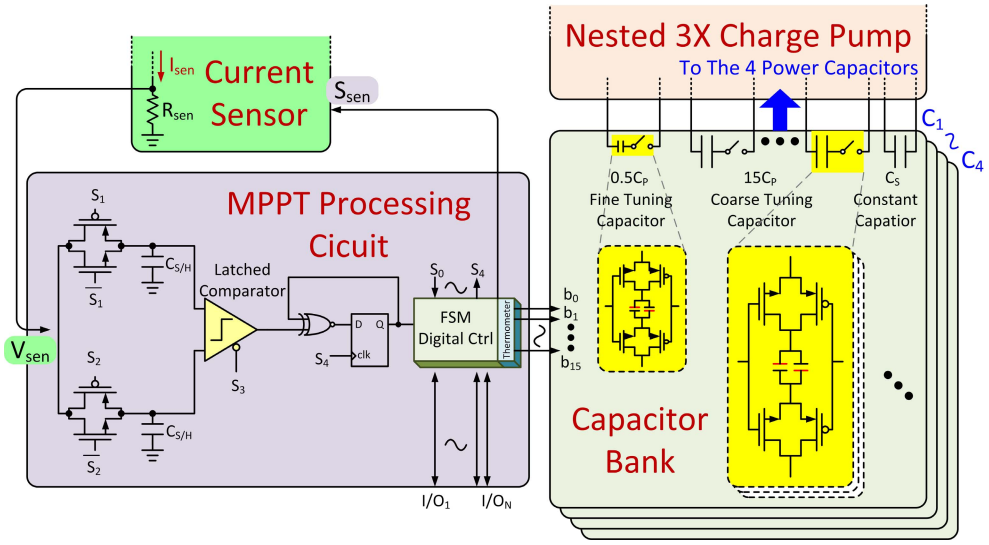
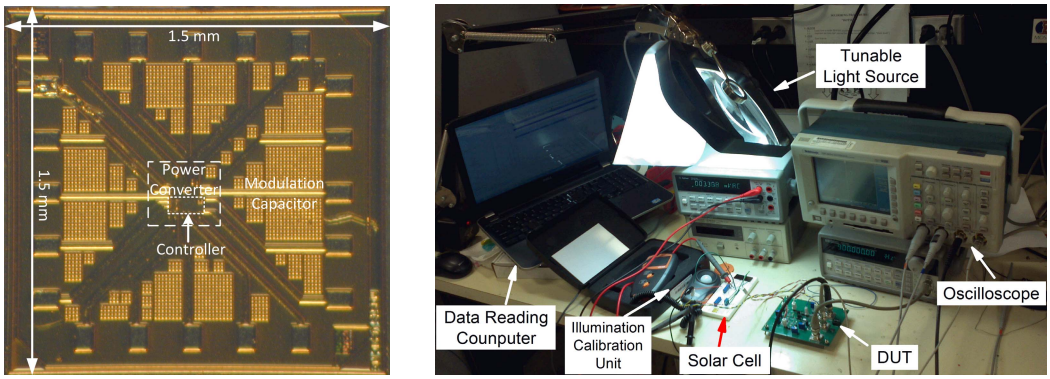


Fig. 12. MPPT processing circuit and capacitor bank.



(a) (b)

Fig. 13. (a) Die photograph of the fabricated chip. (b) Testing setup.

by a potentiometer from 200 kΩ to 10 MΩ paralleled with a 33-mF supercapacitor. The transient V_{solar}, V_{out}, and S_0 are shown in Fig. 14(a). In the beginning, the programmable capacitor bank of the harvesting system was externally preset to an unmatched condition with V_{solar} around 1.06 V. Once S_0 triggered the digital controller, the system began to execute the hill-climbing MPPT procedure step by step from the initial point. After 12 tentative steps, the coarse tuning interval was captured and the fine tuning process quickly narrowed down and locked onto the optimal V_{solar} of 1.18 V. Afterward, the MPPT module was shut down and the controller worked in its minimum power consumption mode. The V_{out} is maintained at 3.1 V with reduced ripples smaller than 10 mV due to the supercapacitor value. As a comparison, a stronger light condition with 800 lux, which emulates a plenty of indoor fluorescence or overcast outdoor daylight, is measured with the results shown in Fig. 14(b). The programmable capacitor bank is preset to the same initial state, which results in a higher unmatched voltage as 1.26 V due to the stronger light condition. Actually, because Z_{cp} is designed to match Z_{solar} as (3) and Fig. 5, the required dynamic range of V_{solar} for high PCE in Fig. 5 does not need as large as 1–1.5 V. For specific application conditions such as $V_{\text{out}} = 3.25$ V in Fig. 5, the necessary dynamic range of V_{solar} for PCE $> 80\%$ is 1.1–1.3 V and is satisfied by the tuning of the programmable capacitor bank. The MPPT procedure only needs two coarse steps to converge at the MPP of 1.24 V. Note that even though the V_{solar} varies from 1.18 to 1.24 V, the corresponding available power changes from 16 to 29 μW.

The practical driving performance of the harvesting system for a temperature sensor and wireless transceiver CC2500 is shown in Fig. 15(a). For saving energy, the loads are operated in a sample-per-second scheme. The sensor and transceiver are turned ON only for 40 ms periodically. The CC2500 reads the monitored temperature data and transmits with a 2.4-GHz RF signal. A computer with an RF receiver reads the environmental temperature data around 27 °C with 0.1 °C sensitivity. The rest 9 s is scheduled as an idle mode. From the transient plot, the harvesting system provides a stable 3.05 V supply and 207 mV ripple voltage. For a comparison, the harvesting performance under different light intensities is demonstrated in Fig. 15(b), which shows that a higher

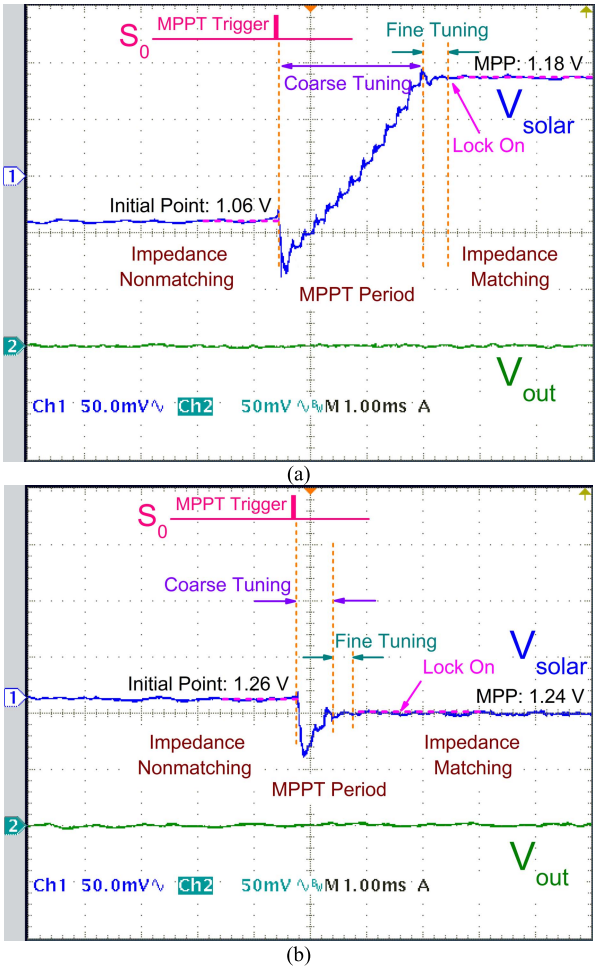


Fig. 14. Experimental transient results of the MPPT procedure under (a) 400 and (b) 800 lux light intensity.

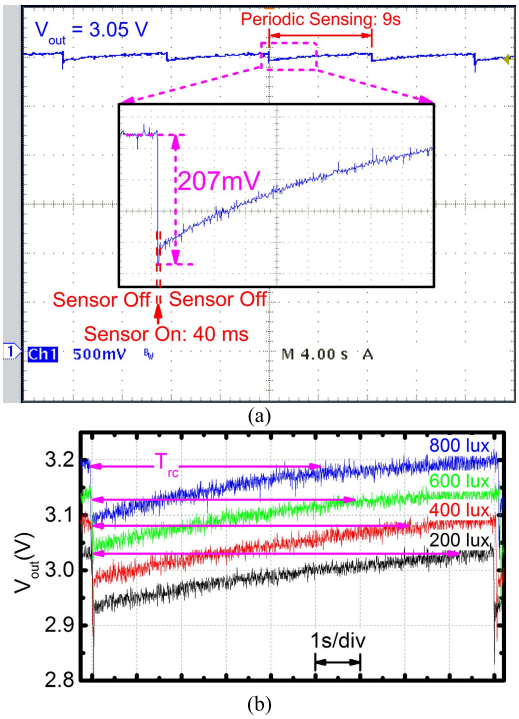


Fig. 15. Experimental transient performance (a) with a wireless temperature sensor operating and (b) comparing one sensing period with different light intensities.

light intensity yields a higher V_{out} and a faster recovering time T_{rc}.

The accuracy of MPP tracking is observed through a static measurement. The MPPT module is disabled, and the capacitor bank is programmed by an external computer through the I/O communication ports. With 3–3.5 V output voltages, the harvested power versus the programmed number N is shown in Fig. 16(a) under different light intensities from 200 to 800 lux. The dynamically captured MPP values are also annotated on the plot for comparison. For all four cases, the harvesting system was able to converge at the global optimal point. The peak PCE without MPPT being activated achieves 92% at 800 lux with the minimized switching loss, the CRL, and the conduction loss. The end-to-end peak PCE with active MPPT versus different PV sources is also demonstrated in Fig. 16(a), in which the harvester maintains efficiencies greater than 80% with output power above 10 μW and output voltage within 3–3.5 V.

The PCE with different light intensities is plotted in Fig. 16(b). The proposed energy harvesting with CR = 3 is specifically designed for the PV cell with nominal $V_{\text{MPP}} = 1.2$ V. For other type of PV cells with nominal V_{MPP} values as 1.5, 1.8, and 2.1 V, the PCE is measured in Fig. 16(b). As analyzed in (3), the resulting $V_{\text{solar}} \times \text{CR}$ significantly deviates from 3 to 3.5 V. Therefore, the CRL ruins the PCE with increasing nominal V_{MPP} or V_{solar}.

The detailed power consumption of the proposed system during MPPT procedure is simulated, as shown in Fig. 17. The current sensor of for MPPT dominates the power consumption; however, it is not necessary to operate all the time. If the FSM initiates the MPPT module after a long time such as several seconds, the energy loss during the small time of MPPT procedure is negligible. When the FSM triggers the MPPT module every 1 s, the output current begins to decrease and the system PCE is degraded to 89%, which can be regarded as the peak dynamic PCE. Further increasing the MPP tracking speed is detrimental to the harvesting system in terms of overall PCE.

Table I compares the performance of the proposed work with other state-of-the-art MPPT harvesters. This harvester uses on-chip switched capacitors and features monolithic integration. The peripheral circuits, including the FSM, the VCO, and the MPPT module, are all powered by the harvester and auxiliary charge pump. Thus, the entire harvesting system is self-sustaining and needs no external bias. The input voltage range is 1–1.5 V, aiming for a single solar cell. For specific V_{out} value between 3 and 3.5 V, the MPPT dynamic range is 200 mV such that $V_{\text{solar}} = 1.1$–1.3 V. The harvested power ranges from 0 to 29 μW depending on the illumination condition. Without MPPT operation under 800 lux intensity, the static end-to-end PCE is 92%. For ordinary operation where the incoming dim indoor light is 400 lux and the MPPT module is operated in the active mode, the dynamic overall PCE can

TABLE I
PERFORMANCE COMPARISON OF LOW-ENERGY HARVESTING SYSTEMS WITH MPPT

	[10]	[20]	[21]	[22]	[17]	This Work
Technology	0.35-μm	0.35-μm	0.25-μm	0.13-μm	0.35-μm	0.18-μm
Fully-integrated	Yes	Yes	No	Yes	No	Yes
Self-sustaining	No	No	Yes	Yes	Yes	Yes
Input Range (V)	2.1-3.5	1-2.7	0.5-2	1.8	1.5-5	1-1.5*
Output Range (V)	3.6-4.4	2	0-5	1.4	0-4	3-3.5
Power Throughput (μW)	100-775	0-80	5-1000	<10	800	0-29
Peak Dynamic PCE with MPPT	67% @529 μW	86% @35 μW	70% @16 μW	58% @10 μW	84.3% @800 μW	88.7% @16 μW

*For specific V_{out}, MPPT dynamic range is 200mV.

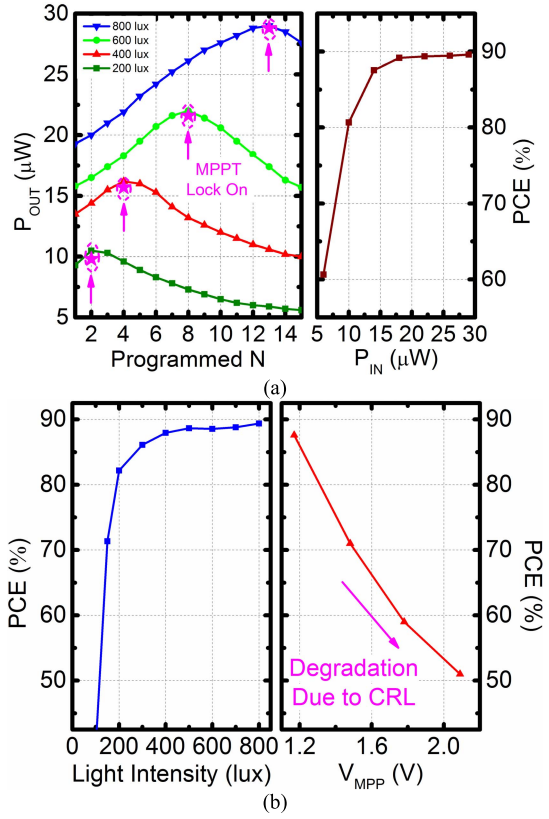


Fig. 16. (a) Static output power with different programmed numbers of the capacitor bank under different light intensities, and end-to-end peak PCE with MPPT versus different PV powers or light intensities. (b) PCE versus light intensity and PCE with different V_{MPP} and CRLs.

achieve a peak value of 89% with 16 μW of throughput power. The proposed harvester achieved a superior performance compared with the reported results, which can only achieve good efficiencies with a large amount of PV power around hundreds of microwatts or harvest a small amount of power below 20 μW but with poor PCE [10], [17], [20]–[22]. In summary, this PV energy harvesting system achieves both ultralow operation capability under 20 μW and excellent self-sustaining PCE of 89% at the same time.

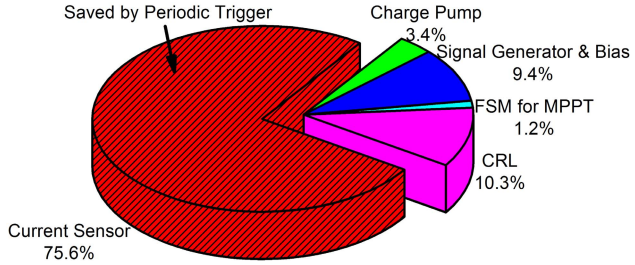


Fig. 17. Detailed power consumption of the PV energy harvesting system.

V. CONCLUSION

This paper proposes a monolithic highly efficient ultralow PV power harvesting system for the smart nodes of IOT networks in 0.18-μm CMOS technology. Instead of commonly used passive RFID supply, the harvesting system offered a higher output power with a compact PV cell as small as 2.5 cm^2. A switched capacitor dc–dc converter is chosen to eliminate the need for an off-chip inductor, making it a monolithic solution suitable for the fully integrated IOT smart nodes. The MPPT function was developed through the hill-climbing algorithm in an energy-efficient approach, ensuring maximum power transfer under various illumination conditions. The capacitor value modulation approach was developed to tune the input impedances of the harvesting system. Compared with the conventional PFM scheme, this modulation scheme had no quiescent power consumption, thus resulting in a higher harvesting efficiency. The experimental results demonstrated that the harvesting system achieves both ultralow operation capability under 20 μW and excellent self-sustaining PCE at the same time. It was able to generate 0–29 μW output power and 3.0–3.5 V output voltages. Given dim indoor light of 400 lux and the MPPT module acting every 1 s, the harvesting system could deliver 16 μW with an end-to-end PCE of 89%. Thus, a temperature sensor and a wireless transceiver were fed by this power in an energy-efficient sample-per-second mode.

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