A Thermal Energy Harvesting Power Supply With an Internal Startup Circuit for Pacemakers

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***Abstract*— A complete thermal energy harvesting power supply for implantable pacemakers is presented in this paper. The designed power supply includes an internal startup and does not need any external reference voltage. The startup circuit includes a prestartup charge pump (CP) and a startup boost converter. The prestartup CP consists of an ultralow-voltage oscillator followed by a high-efficiency modified Dickson. Forward body biasing is used to effectively reduce the MOS threshold voltages as well as the supply voltage in oscillator and CP. The steady-state circuit includes a high-efficiency boost converter that utilizes a modified maximum powerpoint tracking scheme. The system is designed so that no failure occurs under overload conditions. Using this approach, a thermal energy harvesting power supply has been designed using 180-nm CMOS technology. According to HSPICE simulation results, the circuit operates from input voltages as low as 40 mV provided from a thermoelectric generator and generates output voltages up to 3 V. A maximum power of 130 μW can be obtained from the output of the boost converter, which means that its efficiency is 60%. A minimum voltage of 60 mV and a maximum time of 400 ms are needed for the circuit to start up.**

***Index Terms*— Energy harvesting, internal startup, low power, maximum powerpoint trackers, pacemakers, power supplies, thermoelectricity, ultralow voltage.**

I. Introduction

THERE are ∼3 million people worldwide with pacemakers, and every year over 600 000 pacemakers are implanted. Although most people who receive pacemakers are aged 60 years or older, people of any age, even children, may need pacemakers [1].

Most often, a pacemaker is implanted to treat slow heart beating, which is called bradycardia. If the heart beats too slowly, the brain and the body do not get enough blood flow and a variety of symptoms may result [1].

A pacemaker is a small device, about the size of a half dollar piece, implanted just below the collarbone. Although it weighs just about an ounce, a pacemaker contains a powerful battery, electronic circuits, and computer memory that together generate electronic signals. The signals, or pacing pulses, are carried along thin insulated wires, or leads, to the heart muscle.

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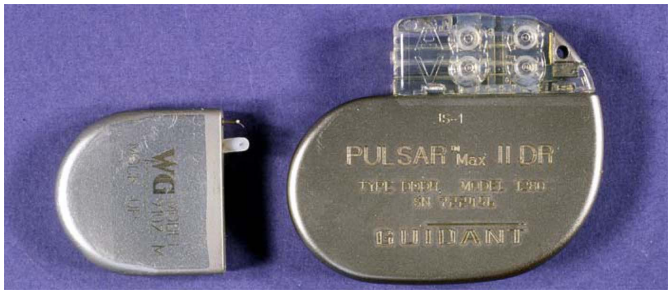


Fig. 1. Pacemaker associated with its battery.

The signals cause the heart muscle to begin the contractions that cause a heartbeat.

One of the main problems about pacemakers is their batteries. As the capacity of the batteries is limited, they limit the lifetime of pacemakers. After a period of five years, one should undergo a surgical procedure to replace the battery of the pacemaker [2]. Replacing these batteries is cumbersome since it requires surgical procedures. In addition, ∼60% of the volume of a pacemaker is taken up by its batteries (Fig. 1). Eliminating these batteries effectively reduces the dimensions of the pacemaker.

One of the alternative methods to power up an implantable pacemaker is harvesting thermal energy. Harvesting ambient thermal energy using thermoelectric generators (TEGs) [3], [4] is a convenient means of supplying power to implantable sensors, especially pacemakers. Micro-TEG is scalable and reliable and does not require any moving parts like vibration energy transducers. As a consequence, it is very appealing in microscale energy harvesting systems, such as human body-powered biomedical devices [5]. Recently, on-chip TE modules have been used to harvest electrical energy from waste heat [6]. As shown in Fig. 2, TEGs (also called Seebeck generators) are devices that convert heat (temperature differences) directly into electrical energy, using a phenomenon called the Seebeck effect (a form of TE effect). A voltage source in series with an internal resistance is a representative of TEGs [7], [8]. The open-circuit output voltage of the TEG is proportional to the temperature gradient. When implanting a TEG, the best place should be as close as possible to the superficial skin, where a maximum temperature difference between the two junctions of the TEG could be established. This would guarantee a good output of the TEG [9].

Using TEGs for implantable applications limits the output voltage to 50 mV for temperature differences of 1–2 K

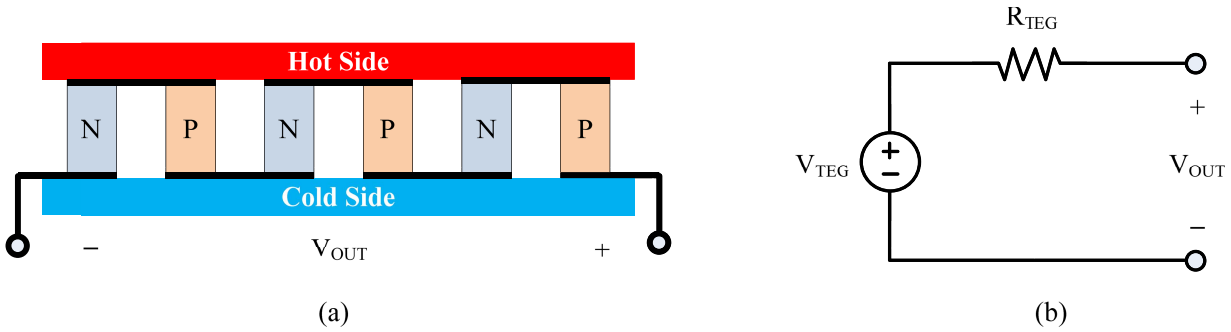


Fig. 2. (a) Typical TEG. (b) Electrical equivalent circuit.

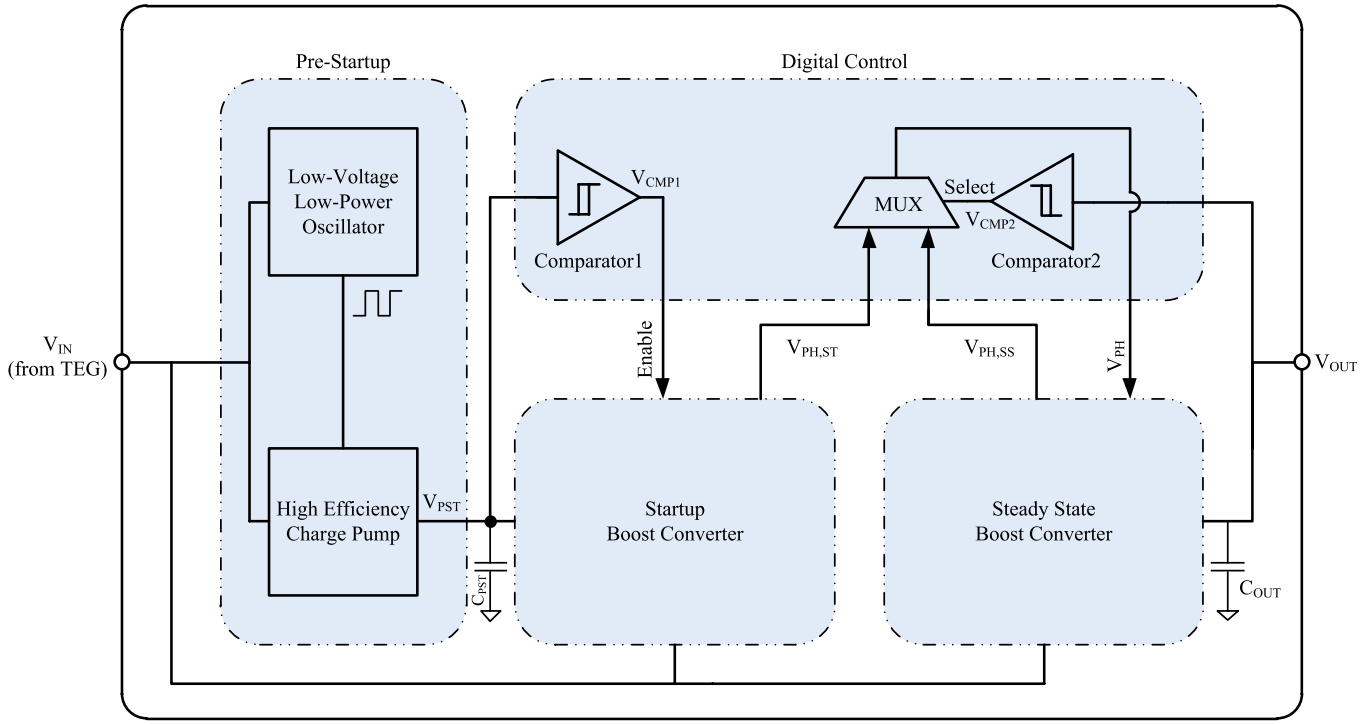


Fig. 3. TE energy harvesting system architecture.

usually found between the body and ambience [10]. This output voltage is very low. A kind of high-efficiency voltage multiplier circuit is then needed to successfully increase the output voltage to the desired value.

In this paper, a voltage multiplier circuit with an internal startup is introduced that successfully converts a minimum of 40-mV input voltage provided from a TEG into a 2.5 V output voltage needed for a pacemaker to operate normally. Typically, pacemakers consume an average of 50 μW at 100% pacing [11]. As a result, the circuit should be able to provide this power. The voltage multiplier circuit is a boost converter based on a constant charge time (CCT) structure as introduced in [12]. Up to now, different approaches have been proposed for starting up a boost converter from low input voltages. Carlson *et al.* [13] have used on-time precharge of the load capacitor to start up the converter. The drawback of this method is that if the storage element is discharged, the boost converter operation fails. Ramadass and Chandrakasan [14] have used a mechanical switch to start up the converter. This method necessarily needs vibration to start up, which is not desirable. This limits the application and increases the cost. Chen *et al.* [10] have proposed a 95-mV startup voltage step-up converter. The 95-mV startup input voltage is somewhat high since the output voltage of a TEG is limited to 40–60 mV. A completely electronic startup step-up converter without using an external voltage is presented in [15]–[17]. The converter proposed in [10] used a transformer with a large turn ratio and is not well suited for.

The rest of this paper is organized as follows. In Section II, the TE energy harvesting system architecture is presented. In Sections III and IV, the circuit implementations of the prestartup charge pump (CP) and the boost converter are described. Simulation results are shown in Section V. Finally, conclusion is given in Section VI.

II. Thermoelectric Energy Harvesting System Architecture

Fig. 3 shows the architecture of the proposed TE energy harvesting system. The output voltage of a TEG is applied to the input of this system. The system works as follows. An ultralow-voltage low-power oscillator generates the required clock phases for a CP system. A high-efficiency

modified Dickson CP is used to increase the input voltage to the extent that is needed for the whole circuit to operate successfully. The output voltage of the TEG is applied to the input of CP. Consequently, CP begins to charge a small internal capacitor (C_{PST}) placed at its output and the capacitor voltage (V_{PST}) begins to rise. When V_{PST} reached a predefined value, the output of the comparator 1 (V_{CMP1}) sets. This enables the startup boost converter (SUBC) to work. The SUBC provides the required clock phases for the steady-state boost converter (SSBC), while the SSBC output voltage (V_{OUT}) does not reach a preset value. When this is achieved, the output of the comparator 2 (V_{CMP2}) sets and the normal operation of the system begins. In this mode, the SSBC itself generates its clock phases. A multiplexer is used to select the source of the required phases for the SSBC based on the V_{CMP2}, whether from SUBC ($V_{\mathrm{PH,ST}}$), or a self-generated one ($V_{\mathrm{PH,SS}}$). In normal operation, the SSBC no longer requires the prestartup CP and SUBC, so it can continue to work on its own. It is designed so that V_{OUT} becomes a regulated output voltage with a low voltage ripple. If, for any reason, V_{OUT} falls out of the range of the output voltage, immediately, the SUBC becomes active and charges the output voltage until it comes within the range. This operation takes time no more than 400 ms. Therefore, the system offers high reliability.

III. Prestartup Charge Pump Structure

A. Low-Voltage Low-Power Oscillator

The output voltage of a TEG is very low. It is not sufficient for conventional oscillators to work properly. Among different types of oscillators, ring oscillators consume less power. A ring oscillator comprises an odd number inverters placed in a loop. The most limiting factor for minimum required supplying voltage of an oscillator, V_{dd}, is its MOS transistor threshold voltage. One way to reduce the MOS threshold voltage is forward body biasing (FBB). The threshold voltage (V_{TH}) of an nMOS transistor relates to its body voltage as follows:

$$V_{\mathrm{TH}} = V_{\mathrm{TH0}} + \gamma\left(\sqrt{|V_{\mathrm{SB}} + 2\Phi_F|} - \sqrt{2\Phi_F}\right) \tag{1}$$

where V_{SB} is the source–body voltage, V_{TH0} is the threshold voltage when $V_{\mathrm{SB}} = 0$, γ is the body effect parameter, and Φ_F is the Fermi potential.

It is observed from (1) that if V_{SB} in nMOS transistors becomes negative, the threshold voltage decreases. Conversely, in pMOS transistors, if V_{SB} has a positive value, the threshold voltage reduces. This technique is called FBB and is frequently used in digital design.

One of the drawbacks of FBB is that it increases the static power consumption of the transistor when it is OFF. This is not disturbing in oscillators since dynamic power consumption dominates static power dissipation. Another problem that arises from FBB is that it turns ON the parasitic bipolar junction transistor (BJT) of MOS. In our design, this is not an issue since the supply voltage of the oscillator is so low that it cannot turn ON the parasitic BJT transistor.

Fig. 4 shows the proposed low-voltage low-power oscillator. In the proposed oscillator, the body terminals of each nMOS and pMOS transistors ($V_{B,\mathrm{nMOS}}$ and $V_{B,\mathrm{pMOS}}$) of each stage are connected to the output voltage of the next stage. Consider two consecutive stages of an oscillator as shown in Fig. 4. When the output voltage of stage $N+1$ ($V_{\mathrm{OUT},N+1}$) goes from low to high state, the output voltage of stage n ($V_{\mathrm{OUT},N}$) has a transition from high to low. As a result, the nMOS transistor of stage N should become ON. As $V_{B,\mathrm{nMOS}}$ is connected to the $V_{\mathrm{OUT},N+1}$, so the body voltage is high and the V_{TH} of the nMOS transistor decreases. This helps the nMOS turning ON faster. The same story happens when stage N has a transition from low to high. The result of the reduction in threshold voltages is a decrease in V_{dd}.

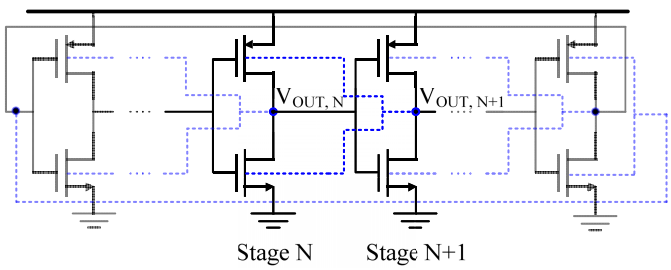


Fig. 4. Proposed low-voltage low-power oscillator.

The detailed circuit schematic of the proposed oscillator is shown in Fig. 5. A minimum of five-stage inverters are needed for the oscillator to start oscillations. The CP needs high-frequency clock signals to quickly charge the output capacitor. To have the highest frequency oscillator, the oscillator is designed with minimum number of stages. In addition, to minimize power consumption, minimum-size inverters are used. The output buffer consists of a chain of inverters. The chain includes eight inverter-based buffers. The sizing of the inverters are shown in Fig. 5 and estimated as in [18].

B. Low-Voltage High-Efficiency Charge Pump

Fig. 6 shows a conventional CP circuit [19]. The circuit comprises two phases. The output voltage of a conventional CP circuit after N stages is

$$V_{\mathrm{OUT}} = V_{\mathrm{IN}} - V_{\mathrm{TH}} + N(V_\Phi - V_{\mathrm{TH}}) \tag{2}$$

where V_{in} is the input voltage, V_Φ is the clock amplitude, and V_{TH} is the threshold voltage of MOS switches.

As is observed from (2), to have a high-efficiency CP, V_{TH} must be minimized. To minimize the threshold voltage, as introduced in Section II, FBB is used. When Φ_1 is low (Φ_2 is high), M_1 (and the following switches of odd stages) is ON. In addition, the output voltage of the even stages are in a high state. Conversely, when Φ_1 is high (Φ_2 is low), M_2 (and the following switches of even stages) is ON. In addition, the output voltage of the odd stages are in a high state. As a result, to have the largest V_{BS} voltage (least V_{TH}) for each transistor (at the time the switch turns ON), the body voltages of the MOS switches of the odd (even) stages should be connected to the output voltage of the last even (odd) stage. This is shown in Fig. 7. Therefore, when M_1 turns ON, its body voltage is in a high state and so its body–source voltage is large. This results in a reduction in threshold voltage.

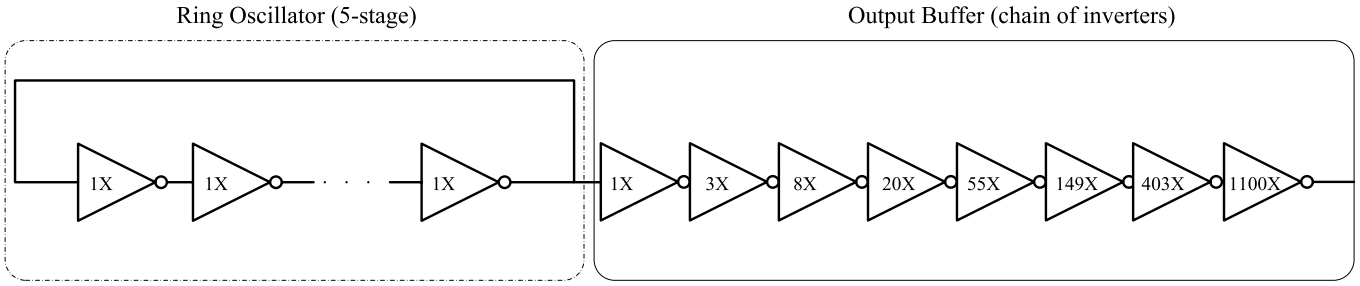


Fig. 5. Structure of the proposed low-voltage oscillator with its output buffer.

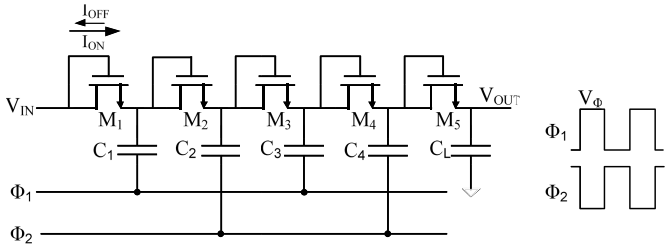


Fig. 6. Conventional CP circuit.

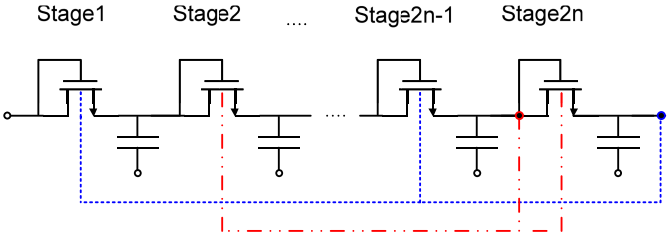


Fig. 7. Proposed low-voltage CP circuit.

Although the threshold voltage has been reduced with this technique, the clock amplitude is still smaller than V_{TH}. However, there still exists the current difference between I_{ON} and I_{OFF} [10], as shown in Fig. 6. This current difference charges the pumping capacitor and pumps up the output voltage. Since the amplitude of the clock provided for the CP is small, the available output current of the CP is limited. Therefore, the output capacitor of the system (C_{OUT}) cannot be placed at the output of the CP since it has a large value. Instead, a small startup capacitor is placed at the output of the CP.

The optimum number of pumping stages is 20 [20] verified by simulation. Lower or higher number of pumping stages may result in a reduction in output voltages or waste energy. As the output voltage provided by this 20-stage CP is not sufficient for the rest of the circuit to operate, as shown in Fig. 8, five 20-stage CPs are cascaded to produce the required output voltage.

IV. Boost Converter Structure

A. Maximum Powerpoint in Boost Converters

Fig. 9 shows a diagram of an ideal boost converter and its equivalent circuit in each phase [21]–[23]. Ashraf and Masoumi [12] have introduced a new Maximum power point tracking (MPPT) method. Maximum power point (MPP) is an operating point in boost converters at which maximum power is delivered to the load. This paper reaches MPP based on maximizing the stored power in the inductor. However, it does not investigate the ON resistances of the switches as well as the series resistance of the inductor. If these parasitic effects are considered, MPP will be changed. The maximum available power that can be delivered to the boost converter is

$$P_{\text{ava,max}} = \frac{V_{\text{TEG}}^2}{4 \times R_{\text{TEG}}}. \tag{3}$$

The average power (P_{avg}) stored on the inductor is as follows:

$$P_{\text{avg}} = \frac{E_L}{T_{\text{rise}}} = \frac{0.5 \times L \times i_{\text{max}}^2}{T_{\text{rise}}} \tag{4}$$

where L is the value of the inductor and i_{max} is the inductor current at the end of phase Φ_1, i.e., T_{rise}. The current i_{max} can be calculated as

$$\begin{aligned} i_{\text{max}} &= i(t = T_{\text{rise}}) \\ &= \frac{V_{\text{TEG}}}{R_S + R_{\text{ON}} + R_{\text{TEG}}} \left(1 - e^{-\frac{R_S + R_{\text{ON}} + R_{\text{TEG}}}{L} \cdot T_{\text{rise}}}\right) \end{aligned} \tag{5}$$

where R_S is the series resistance of the inductor and R_{ON} is the ON resistance of switch S_1. Substituting (5) in (4) yields

$$P_{\text{avg}} = \frac{E_L}{T_{\text{rise}}} = \frac{L \cdot V_{\text{TEG}}^2 \left(1 - e^{-\frac{R_S + R_{\text{ON}} + R_{\text{TEG}}}{L} \cdot T_{\text{rise}}}\right)^2}{2 \cdot T_{\text{rise}} \cdot (R_S + R_{\text{ON}} + R_{\text{TEG}})^2}. \tag{6}$$

The average power is maximized when T_{rise} is as follows:

$$\frac{dP_{\text{avg}}}{dT_{\text{rise}}} = 0 \Rightarrow T_{\text{rise}} = 1.256 \times \frac{L}{(R_S + R_{\text{ON}} + R_{\text{TEG}})}. \tag{7}$$

Therefore, the maximum average power stored in the inductor can be calculated as

$$\begin{aligned} P_{\text{avg,max}} &= \frac{E_L}{T_{\text{rise}}} = \frac{L \cdot V_{\text{TEG}}^2 \left(1 - e^{-\frac{R_S + R_{\text{ON}} + R_{\text{TEG}}}{L} \cdot T_{\text{rise}}}\right)^2}{2 \cdot T_{\text{rise}} \cdot (R_S + R_{\text{ON}} + R_{\text{TEG}})^2} \\ &= 0.2036 \times \left(\frac{V_{\text{TEG}}^2}{R_S + R_{\text{ON}} + R_{\text{TEG}}}\right). \end{aligned} \tag{8}$$

The relative value of the $P_{\text{avg,max}}$ and $P_{\text{ava,max}}$ will be as follows:

$$\frac{P_{\text{avg,max}}}{P_{\text{ava,max}}} = 0.8145 \frac{R_{\text{TEG}}}{R_S + R_{\text{ON}} + R_{\text{TEG}}}. \tag{9}$$

Equation (9) states that under the best conditions ($R_S + R_N \ll R_{\text{TEG}}$), the maximum average power that can be

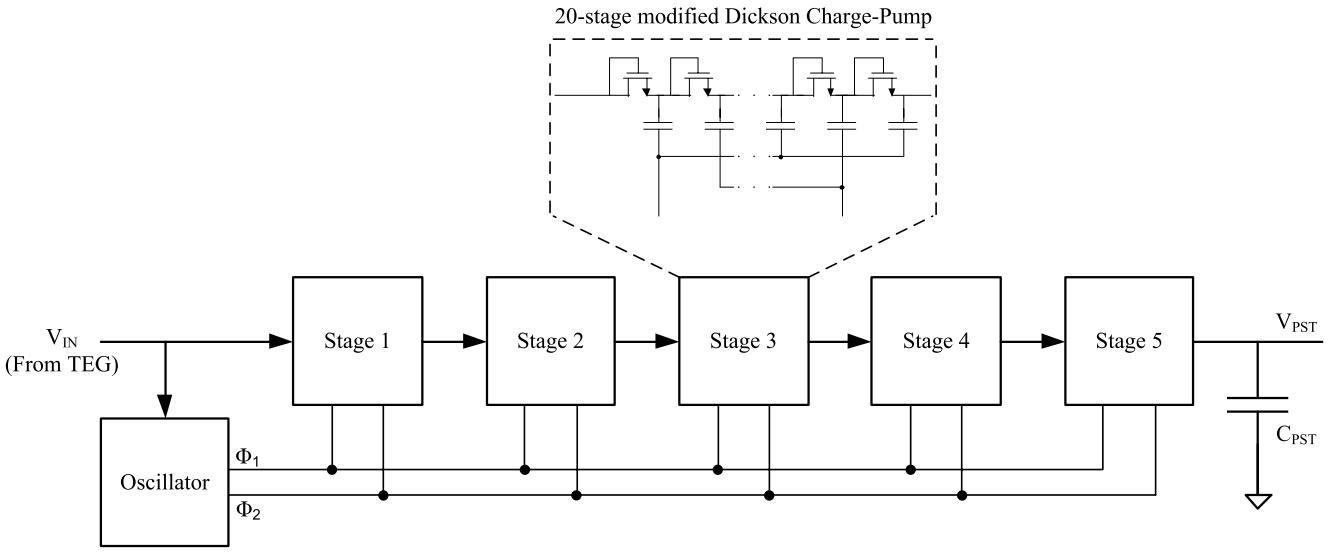


Fig. 8. Structure of the prestartup circuit.

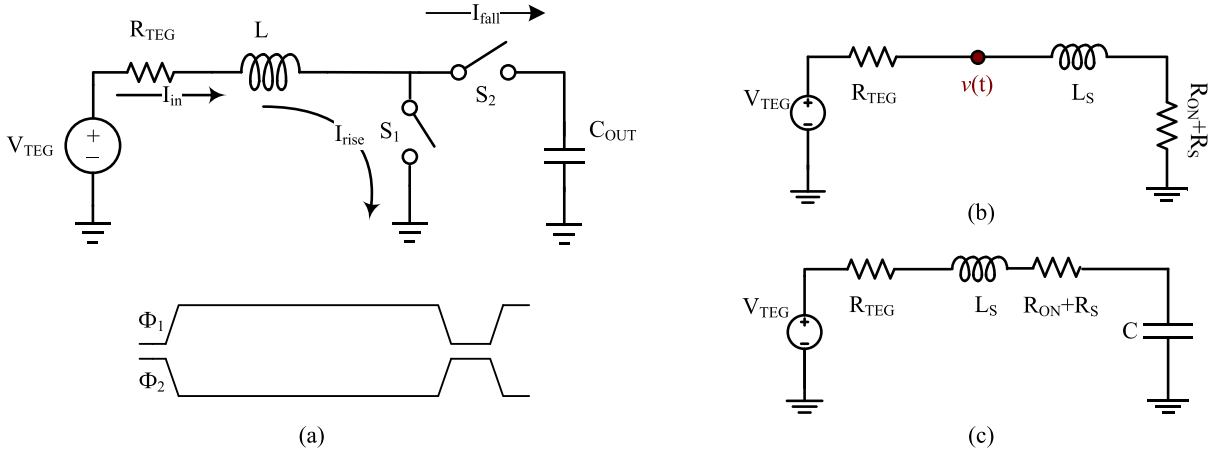


Fig. 9. (a) Ideal boost converter and its phases. (b) Equivalent circuit in phase Φ_1. (c) Equivalent circuit in phase Φ_2.

stored on the inductor is $\sim 0.8\times$ of the available power from source. To maximize $P_{\text{avg,max}}$, R_S and R_{ON} must be designed to satisfy the $R_S + R_{\text{ON}} \ll R_{\text{TEG}}$ criterion. To minimize R_{ON}, the size of the switch must be maximized. Larger switches result in more dynamic power dissipation. This tradeoff must be considered at the design time.

The input voltage of the boost converter, $v(t)$, at MPP should be

$$\begin{aligned} v(t = T_{\text{rise}}) &= V_{\text{TEG}} - R_{\text{TEG}} \times i(t) \\ &= V_{\text{TEG}}\left(1 - \frac{0.71 \times R_{\text{TEG}}}{R_S + R_{\text{ON}} + R_{\text{TEG}}}\right) \\ &= V_{\text{TEG}}\left(\frac{R_S + R_{\text{ON}} + 0.29R_{\text{TEG}}}{R_S + R_{\text{ON}} + R_{\text{TEG}}}\right). \end{aligned} \quad (10)$$

Fig. 9(c) shows the boost converter in the second phase, Φ_2. To transfer maximum power from the inductor to the capacitor (and hence to the load), Φ_2 must be stopped when the inductor current reaches zero. If the inductor current become zero, will be equal to T_{fall} as

$$T_{\text{fall}} = \frac{2L\sqrt{C}}{\sqrt{4L - CR^2}} \arctan\left(\frac{-1}{3R} \times \frac{\sqrt{4L - CR^2}}{\sqrt{C}}\right) \quad (11)$$

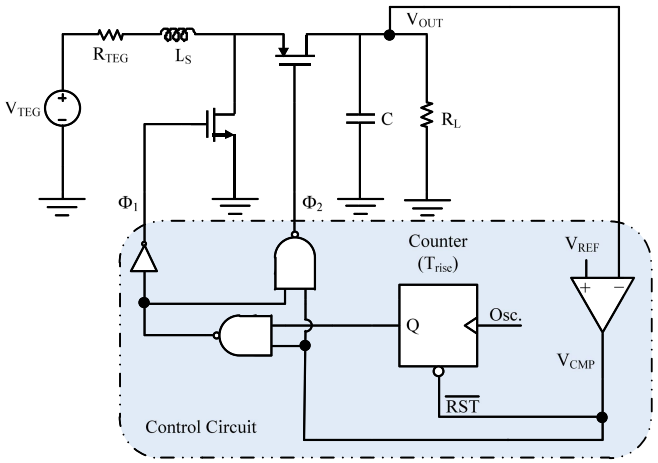


Fig. 10. CCT structure [12].

where R is the sum of the R_{TEG}, R_S, and R_{ON}. As is observed from (11), T_{fall} has a constant value. Besides, the output voltage of a boost converter is calculated as

$$V_{\text{OUT}} = V_{\text{IN}} \frac{T_{\text{rise}} + T_{\text{fall}}}{T_{\text{fall}}}. \quad (12)$$

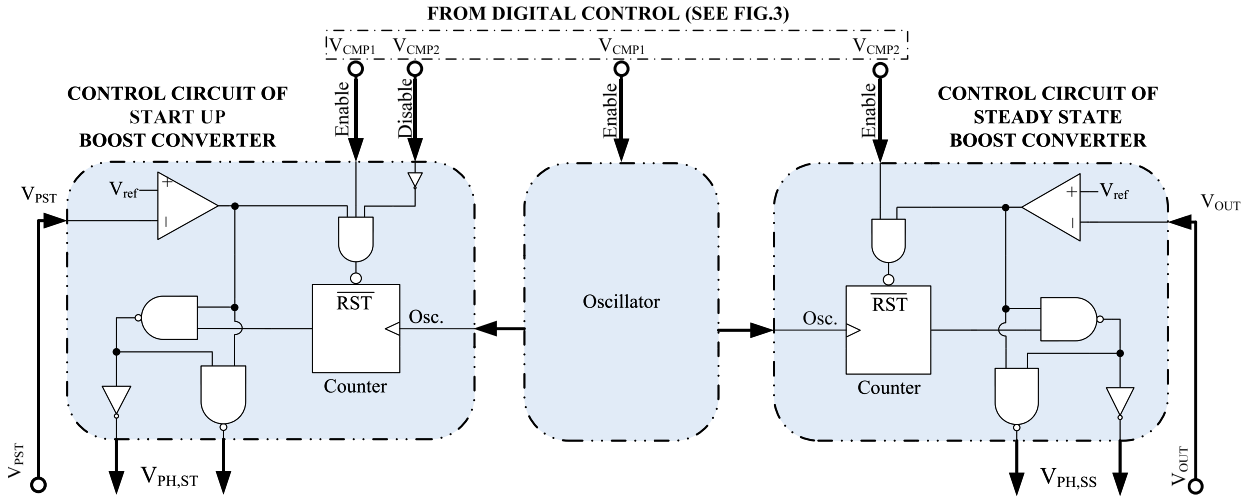


Fig. 11. Structure of the control section of boost converters.

It can be observed from (12) that a small change in the input voltage or load leads to a large change in the output voltage. This will lead to nonregulated V_{OUT} [12]. To control V_{OUT}, Φ_2 can be stopped before the inductor current reaches zero. If the load is small, Φ_2 is stopped sooner. If a heavy load is used, Φ_2 is stopped later. The maximum allowable load for the boost converter is defined when all of the power of the inductor is transferred to the capacitor. In this way, the inductor current become zero at the end of Φ_2.

B. System Architecture

The system architecture of the proposed boost converter is shown in Fig. 10 and is based on the CCT structure [12]. In this scheme, the modified MPPT is employed and maximum available power can be drawn from the input source [12]. T_{fall} is adjusted so that the output voltage is set to an arbitrary value. A comparator is used to compare the output voltage with the desired output value. When the output voltage becomes less than the ideal value, a counter starts to count and its output as well as Φ_1 rises to a high state. The counter continues counting until T_{rise} as in (7) is reached. After that, the output of the counter becomes low. As a result, phase 1 falls to a low state and conversely, Φ_2 changes to a high state. The phase Φ_2 remains high until the output voltage becomes greater than the desired voltage. In this way, the output voltage is regulated to the desired value. The generated output voltage is used as the power supply for the control circuit [12].

To minimize the power consumption of the control circuit, it is turned OFF whenever it is not needed. As illustrated in Section II, when the system is in prestartup state, the SUBC and the SSBC are in the stand-by mode. Hence, the oscillator of the control circuit of these parts does not need to oscillate. As shown in Fig. 11, the output of the comparator 1 controls the activity of the oscillator. When V_{CMP1} is low, the oscillator is inactive. When it becomes high, the oscillator starts its operation. As the SUBC and the SSBC both need a similar oscillator, one oscillator is shared between them to reduce power consumption.

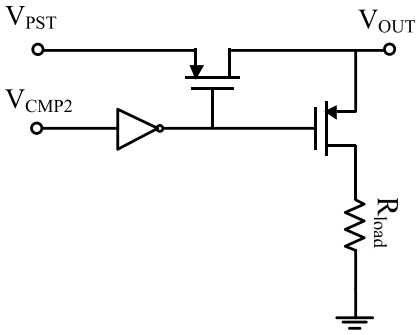


Fig. 12. Circuit used to short V_{PST} and V_{OUT}, and to detach the load from V_{OUT}.

To enable the control circuit of the SSBC, the output of V_{CMP2} is connected to the reset of the counter. As long as the output voltage has not reached its final value, V_{CMP2} is low and the counter is in the reset mode. When the output voltage has passed its final value, V_{CMP2} sets and the counter starts to count. Once the SSBC is enabled, there is no need for an SUBC. Therefore, to minimize power dissipation, the control circuit of the SUBC must be disabled. This is done using a disabling circuit for the control circuit of the SUBC (Fig. 11). Note that if the control circuit of the SUBC is disabled, there is no control on V_{PST}. To keep V_{PST} in the range so that V_{CMP1} remains high, while the circuit is in the steady-state mode, C_{PST} and C_{OUT} are shorted together (Fig. 12). When the circuit is in the startup mode, the load circuit should not be connected to the output. As shown in Fig. 12, to detach the load from V_{OUT} while the circuit is in the startup mode, a pMOS switch is used which is controlled by V_{CMP2}.

Since both the SUBC and the SSBC are connected to a single input node (output voltage of TEG), if the input is not disconnected from the SUBC in the steady-state mode, there is a current leakage through the SUBC and MPPT cannot be employed effectively for the SSBC. Fig. 13(a) shows the connections of a single TEG to the SUBC and the SSBC and the current leakage. To detach the SUBC from TEG, one way is to place a switch (S_3) between the TEG and the SUBC which is controlled by V_{CMP2} [Fig. 13(b)]. This is not efficient,

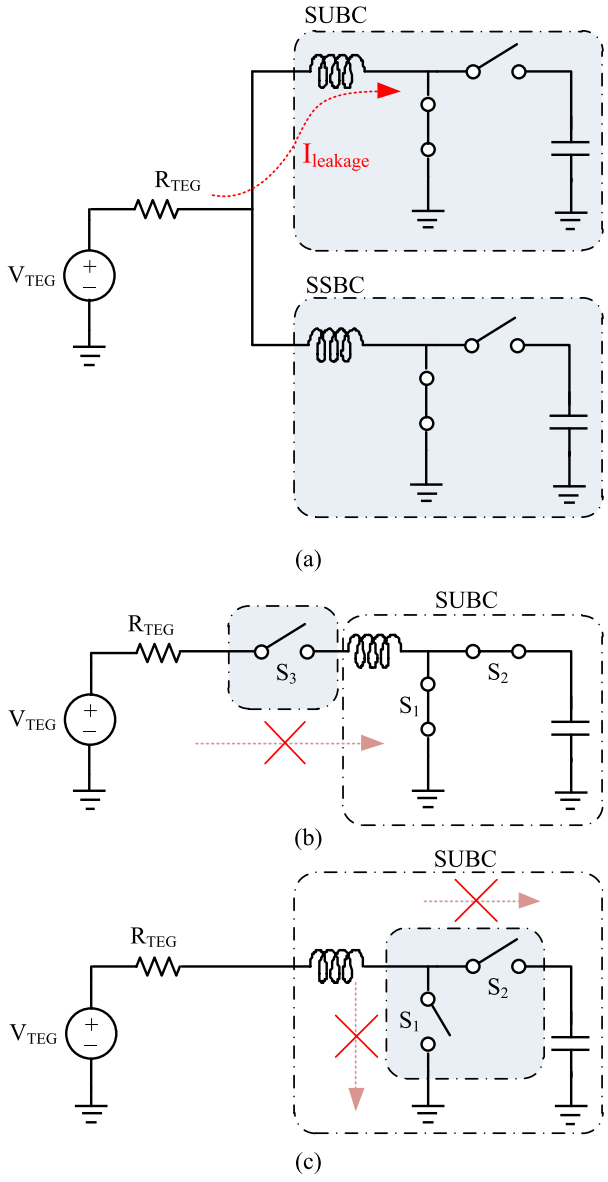


Fig. 13. SUBC input isolation approaches. (a) Current leakage of SUBC in the steady-state mode. (b) Placing an extra switch S_3 to detach SUBC. (c) Turning OFF S_1 and S_2 to detach SUBC.

since this extra switch introduces losses and lowers the overall system efficiency. Instead, as shown in Fig. 13(c), another way is to turn OFF both switches of S_1 and S_2 in the SUBC by means of its voltage phases ($V_{PH,ST}$). This successfully disconnects the SUBC from the whole circuit.

The output of this system is capable of providing a limited specified maximum power. If the load consumes more power, the output voltage tends to decrease, and if it is not controlled correctly, the whole system will fail. To improve system reliability, first, the comparators are designed to have a hysteresis loop. Since V_{OUT} and V_{PST} have ripples, the hysteresis loops of these comparators prevent the oscillations of V_{CMP1} and V_{CMP2}. Second, the low threshold level of comparator 1 and comparator 2 ($V_{TH,L,CMP1}$ and $V_{TH,L,CMP2}$) are set differently. $V_{TH,L,CMP2}$ is set higher than $V_{TH,L,CMP1}$. In this way, when V_{OUT} falls below $V_{TH,L,CMP2}$, V_{CMP2} resets to zero and the system state will change to the startup

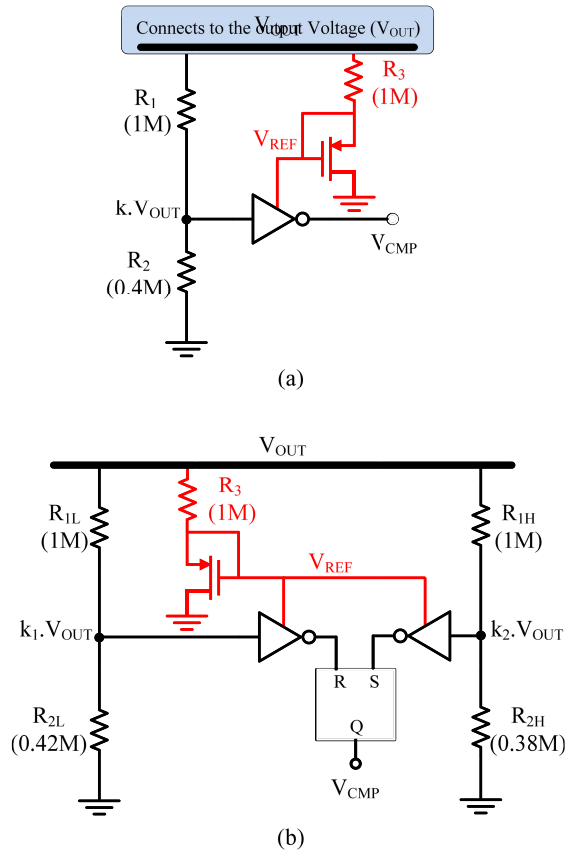
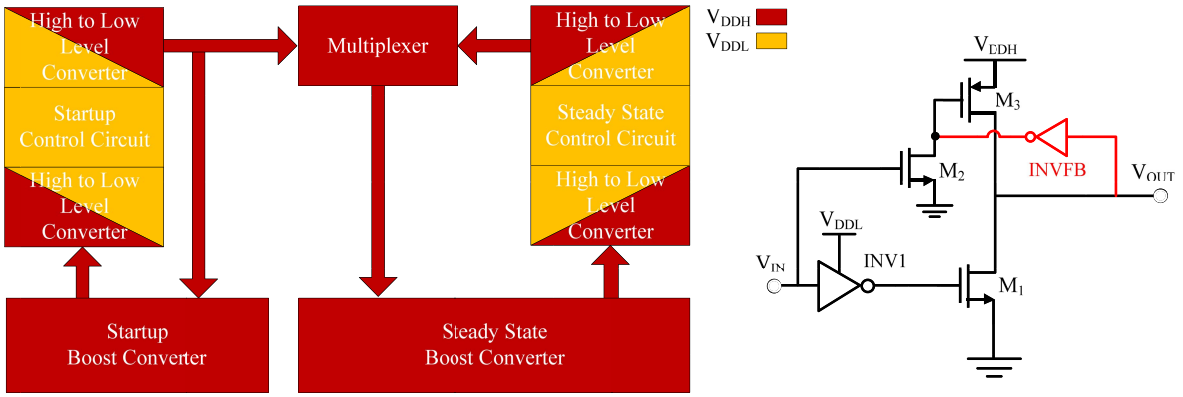


Fig. 14. (a) Schematic of the low-power self-reference comparator. (b) Proposed self-reference hysteresis comparator. Values are for SSBC comparators.

mode. In addition, the load is disconnected from the whole circuit. In the startup mode, the system charges C_{OUT} again and V_{OUT} rises. Having used this technique, the system will never fail.

C. Self-Reference Hysteresis Comparator

Fig. 14(a) shows a comparator circuit introduced in [12]. A pMOS transistor with its gate and source terminals connected to each other is used. This transistor operates in the subthreshold region and has a constant current. This constant current flows through a resistor and builds a reference voltage. The generated reference voltage is used as the supply of an inverter. A percentage of output voltage ($k \cdot V_{OUT}$) is applied to the input of the inverter. Using this method, if the output voltage is larger than a desired value, then the output of the comparator (V_{CMP}) becomes low. The relative values of R_1 and R_2 set the threshold level of the comparator [12]. Process variations of the pMOS threshold voltage can be compensated for by the resistive divider which are discrete components. In addition, the proposed reference generator does not suffer much from temperature variations in this application since the pacemaker needs to be implanted in the body. The temperature variations inside the body are about ± 1 °C. These variations do not impact on the generated reference voltage since the temperature coefficient of the proposed circuit is about -2 mV/°K.



(a) (b)

Fig. 15. (a) Insertion of level converters to lower the power dissipation of digital sections. (b) Low-to-high level converter circuit [12].

Fig. 14(b) shows the proposed hysteresis comparator. Two sets of resistors (R_{1L} and R_{2L}, R_{1H} and R_{2H}) set the low and the high threshold levels of two comparators. To create a hysteresis loop for the comparator, an RS flip-flop is used. The reset input of the flip-flop is connected to the output of the low-threshold comparator, while the set input is adjoined to the high-threshold one. When the output voltage passes the high threshold voltage, the RS flip-flop sets. On the other hand, the flip-flop will not reset until the output voltage falls below the low threshold voltage.

D. Level Converter

To minimize the power consumption of the digital section, a level converter circuit is used. As shown in Fig. 15(a), the level converter converts the output voltage of the boost converter to (V_{DDH}) to the least voltage (V_{DDL}) that is required for the control circuit to operate properly. The generated voltage phases are then up-converted into V_{DDH} level to minimize the switch losses. A high-to-low level converter is used to convert the output voltage of the comparator into a lower voltage. Conversely, a low-to-high level converter is used to convert the constructed voltage phases into a higher voltage. The structure of the level converter circuit is shown in Fig. 15(b) [12].

E. Counter

As is observed from (7), T_{rise} has a constant value. It is set externally by means of a counter to reach MPP. Edge-triggered D flip-flops with asynchronous reset [24] (Fig. 16) are used to realize the counter. The output of the comparator is connected to the reset of the counter. When the output voltage becomes less than the desired voltage, the output of the comparator becomes high and this enables the counter to start counting. As soon as the output voltage becomes more than the desired value, the counter resets. Eight D flip-flops are arranged successively to realize the counter. This configuration has low power consumption since the clock frequency of every stage is half that of its preceding stage.

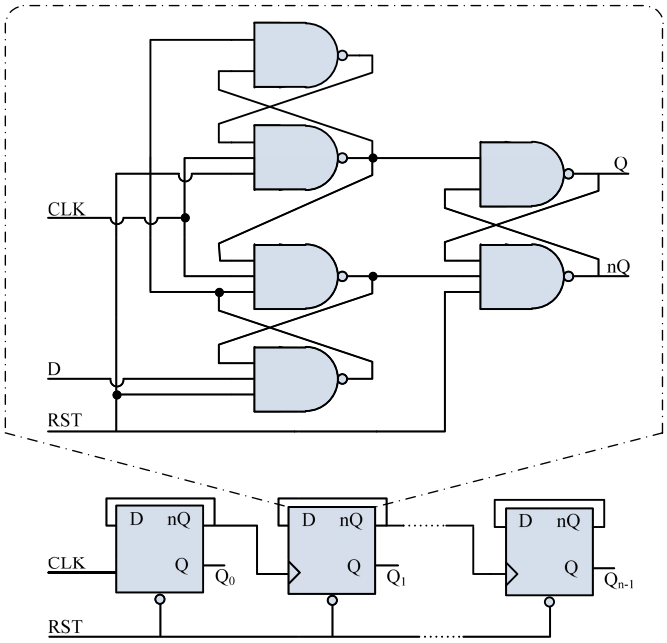


Fig. 16. Configuration of the counter and edge-triggered D Flip-flop with asynchronous reset [24].

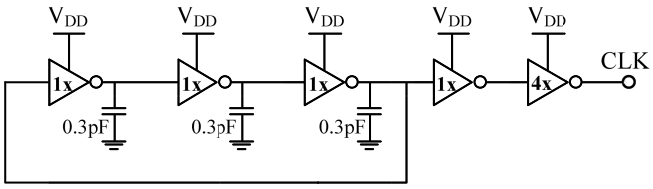


Fig. 17. Configuration of the boost converter oscillator.

F. Boost Converter Oscillator

The counter shown in Fig. 16 needs a clock signal. A ring oscillator, as shown in Fig. 17, is used to generate the required clock phases. To minimize power consumption, three inverter-based stages are used to realize the oscillator. The on-chip capacitors adjust the frequency of the oscillations which is ~1 MHz. A Two-stage buffer is used at the output of the oscillator to successfully drive the counter.

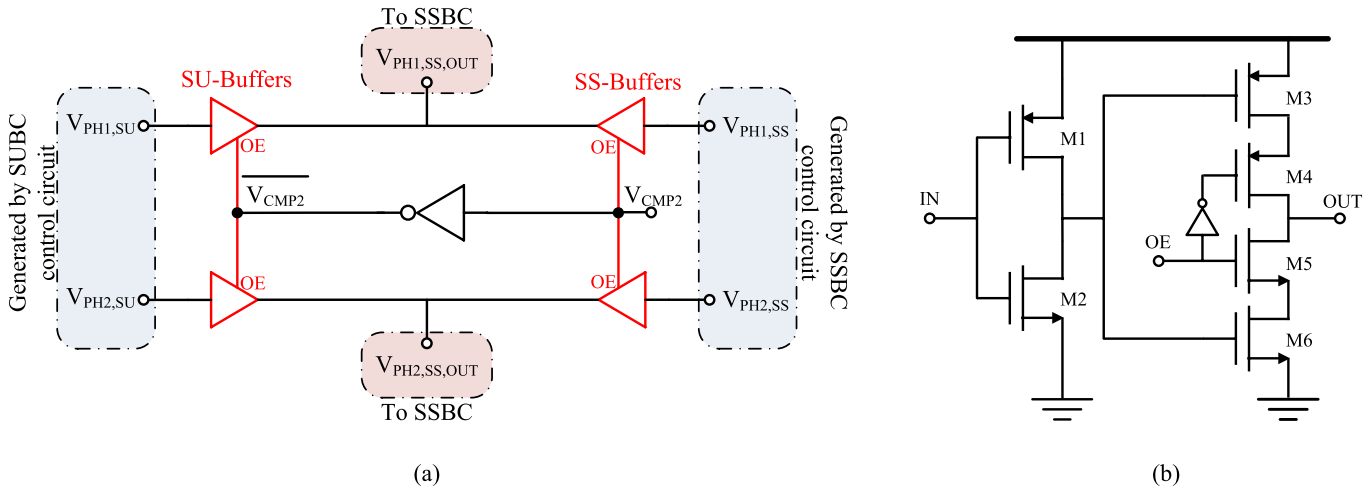


Fig. 18. (a) Schematic of multiplexer. (b) Schematic of a tristate buffer [25].

G. Multiplexer

Fig. 18(a) shows the schematic of the multiplexer. The function of the multiplexer is to determine whether the clock phases for the SSBC are provided from the SUBC or generated from itself. The multiplexer is composed of two tristate buffers [25] whose outputs have wired-OR configuration. The output enable (OE) of one of the buffers (SS-Buffer) is connected to V_{CMP2}. Conversely, the OE of the other buffer (SU-Buffer) is connected to the inverse of V_{CMP2}. The input of SU-Buffer (SS-Buffer) is connected to the generated clock phases of the SUBC (SSBC). When the circuit is in the startup mode, V_{CMP2} is zero, so SU-Buffers will be active. As a result, the clock phases are provided from the SUBC. When V_{CMP2} sets, SS-Buffers will be active and the clock phases for the SSBC are generated by itself. Two multiplexers are used for $V_{\Phi 1}$ and $V_{\Phi 2}$. The schematic of a tristate buffer is shown in Fig. 18(b). An inverter is followed by a tristate inverter to create the tristate buffer. M_4 and M_5 form the OE of the inverter. If OE is low, M_4 and M_5 are OFF, so the output is high impedance. If OE is high, M_4 and M_5 are on and the tristate inverter acts like a traditional inverter.

V. Simulation Results

To evaluate the proposed structure, a thermal energy harvesting power supply is designed and simulated in HSPICE using 180-nm CMOS technology. The designed power supply is used as the supply for a pacemaker. The pacemaker power consumption is 50 μW and its supply voltage is 2.5 V [11]. Therefore, the boost converter should convert the input voltage of the TEG into 2.5 V and delivers at least 50 μW to the load.

A 40-mV input voltage source with a 1.5-Ω internal resistance [26] is applied to the input of the circuit and the output voltage is measured when connected to a resistive load. This resistive load is an equivalent circuit for the pacemaker.

The circuit parameters are listed in Table I. The values of the capacitor and the inductor are chosen in such a way that the requirements of the output voltage are met. The inductors are discrete components and their sizes are compliant with Surface Mount Device packages. The sizes of the nMOS and pMOS switches are defined to meet MPP as well as to minimize the overall static and dynamic power consumption.

TABLE I
Values of Circuit Parameters

Parameters	Symbol	Value
Input Voltage	V_{TEG}	40 mV
Source Resistance	R_{TEG}	1.5 Ω
Output Voltage	V_{OUT}	2.5 V
Load	R_{L}	50 kΩ (min)
Inductor (startup boost converter)	L_{ST}	100 uH
Inductor (steady state boost converter)	L_{SS}	400 uH
Output Capacitor	C_{OUT}	400 nF
Pre-startup Capacitor	C_{PST}	5 nF
NMOS Switch Size (W/L)	S_1	100u×100/350n
PMOS Switch Size (W/L)	S_2	1u×1/350n

Fig. 19(a) shows the output of the proposed oscillator. The minimum supplying voltage for this oscillator is 70 mV. To further reduce V_{dd}, midthreshold MOS transistors are used. This results in reduction in V_{dd} down to 60 mV.

The output of the oscillator is fed to the proposed CP and its resulting output is shown in Fig. 19(b). As seen in the figure, after ∼8 s, the output of the prestartup circuit reaches 2.5 V. Whereas this is a long duration, it happens just once at power ON of the system (hence it is called prestartup). After V_{PST} reaches 2.5 V, the output of comparator 1 sets and the prestartup circuit is disconnected from the whole circuit. This unit remains in the system just to increase the system performance reliability.

Fig. 20 shows how the system works. As V_{PST} reaches $V_{\mathrm{TH,H,CMP1}}$, V_{CMP1} sets, the prestartup circuit is disconnected from C_{PST}, and the oscillator and the control circuit of SUBC become active. The control circuit provides the required clock phases, Φ_1 and Φ_2, for both itself and the SSBC. As a result,

TABLE II
COMPARISON OF THE PROPOSED STRUCTURE WITH SOME EMERGING TECHNOLOGIES

References	Technology	Minimum input Voltage	Output Voltage	Maximum Output Power	Conversion Factor	Startup voltage/ method	Efficiency for maximum conversion factor	MPPT
[10] (measurement)	65 nm	100mV	0.8-1V	2mW	8-10	95mV / Internal (Capacitor pass on)	n/a	NO
[13] (measurement)	130 nm	20mV	1 V (regulated)	10 uW	50	650mV / External (Precharge)	46% (end-to-end) (Vin=20mV)	NO
[14] (measurement)	350 nm	25mV	1.8 V (regulated)	10 uW	72	35mV / Internal (Mechanical SW)	40% (end-to-end) (Vin=25mV)	YES
[27] (measurement)	350 nm	1V	1.75-4.3V	n/a	1.75-4.3	1V / Internal (n/a)	5% (boost converter) (Vout=4.3V)	NO
[28] (measurement)	350 nm	0.6V	2V	1mW	3.3	1.28V / External (Battery)	20% (end-to-end) (Vin=0.6V)	YES
This Work (Post Layout Simulation)	**180 nm**	**40 mV**	**1-3 V (regulated)**	**130 uW**	**20-75**	**60 mV / Internal (Oscillator + CP)**	**boost converter: 59% end-to-end: 48% (Vin=40mV)**	**YES (modified)**

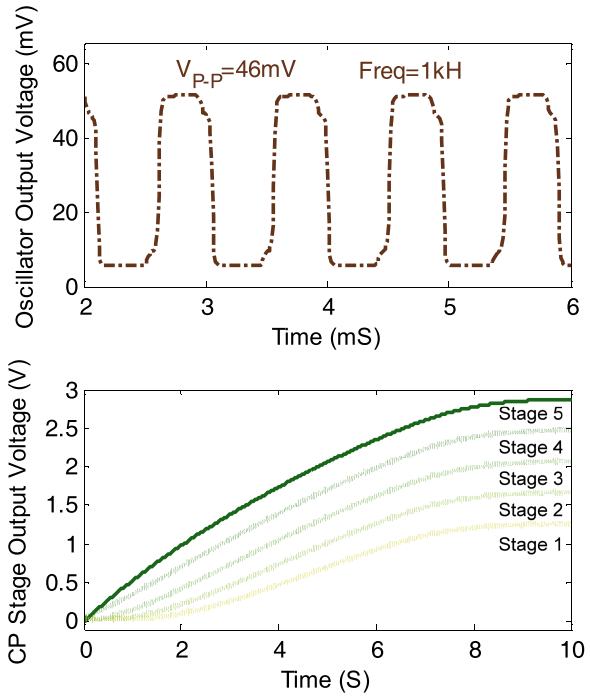


Fig. 19. (a) Output of the proposed low-voltage oscillator ($V_{dd} = 60$ mV). (b) Output voltages of the prestartup CP stages.

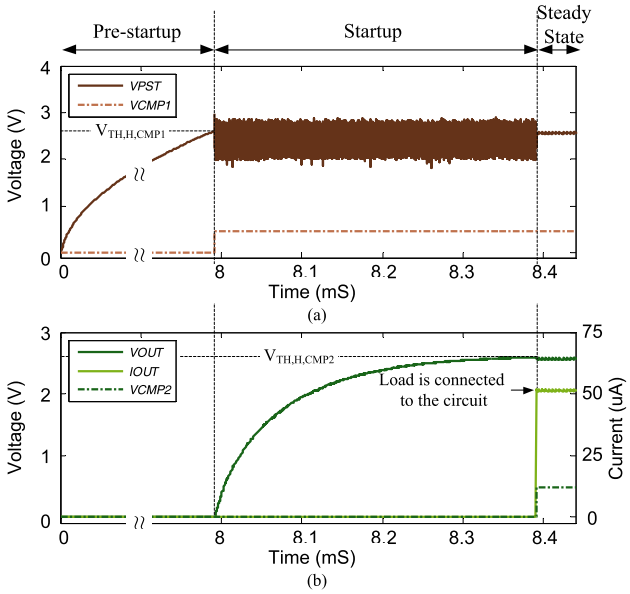


Fig. 20. (a) Waveform of the prestartup voltage associated with the output voltage of comparator 1. (b) Waveform of the output voltage associated with the output voltage of comparator 2 and the load current.

the voltage on C_{PST} remains almost constant, and the voltage on C_{OUT} rises. V_{OUT} rises until it reaches $V_{TH,H,CMP2}$. When this is achieved, V_{CMP2} sets, and the multiplexer disconnects the clock phases of the SUBC from the SSBC and lets the SSBC to generate the clock phases for itself. From this time, the system can provide the required power for the pacemaker. The comparator high and low threshold voltages are set to be 2.6 V and 1.5 V for comparator 1 and 2.6 and 2.5 V for comparator 2, respectively. V_{PST} has a high ripple, so the hysteresis window of comparator 1 should be designed wide enough.

Fig. 21(a) shows the output voltage of the system under no load and full load conditions. Under no load condition, the average output voltage is 2.56 and the output voltage ripple is <50 mV (<2%). Full load condition results in the average output voltage of 2.52 with 50-mV output voltage ripple. Note that in both conditions, the pulsewidth of $V_{\Phi 1}$ is constant, but its period changes [Fig. 21(b)]. This verifies that the boost converter always operates in MPP under any load conditions.

The circuit is able to provide the desired output voltage when the load consumes no more than 130 μW. If the load power consumption exceeds this value, as shown in Fig. 22, the output tends to decrease. As described in Section IV, the circuit mode is changed to the startup mode and the load is detached from the whole system. In the startup mode, the circuit charges V_{OUT} until V_{CMP2} is set. The circuit enters the steady-state mode again and normal operation of the circuit is retrieved.

Table II gives a summary of the simulation results of the proposed structure and also a comparison between the proposed architecture and some state-of-the-art energy harvesting circuits. Although the results from other references are

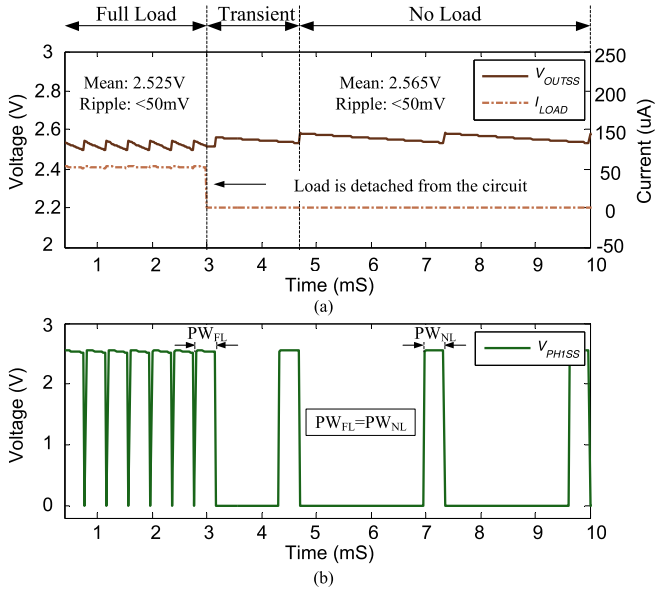


Fig. 21. Full load and no load conditions. (a) Waveform of the output voltage associated under full load and no load conditions. (b) Waveform of phase Φ_1. The pulsewidth of Φ_1 remains constant.

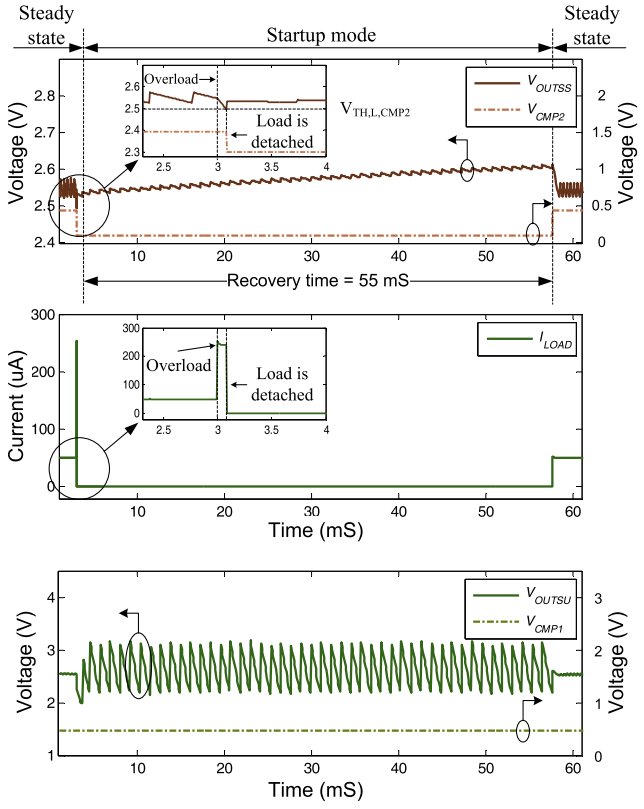


Fig. 22. Recovery procedure when overload occurs. Before $t = 3$ ms, the circuit is in the steady-state mode. At $t = 3$ ms, overload occurs. The output voltage starts to decrease. When the output voltage reaches $V_{TH,L,CMP2}$ (2.5 V), V_{CMP2} resets, the load is detached, and the circuit mode is changed to the startup mode (Note that V_{CMP1} remains set since $V_{TH,L,CMP1}$ is set to 1.5 V). In the startup mode, the circuit charges V_{OUT}. When V_{OUT} reaches $V_{TH,H,CMP2}$ (2.6 V), the circuit enters the steady-state mode again.

experimental results, real models from the technology file are used for elements in the proposed circuit which is simulated in HSPICE. In addition, all parasitics are considered using a postlayout extraction process. It is obvious that there will be some degradation in measurement results, but this idea makes some improvements in efficiency as well as startup voltage. The proposed converter gains 48% end-to-end efficiency for its maximum conversion factor, which is the highest efficiency among the selected state-of-the-art references. The new structure uses a modified MPPT scheme that increases the overall system efficiency. In addition, the proposed converter has the highest conversion factor. In addition, the proposed converter has the minimum startup voltage with which its fabrication is CMOS compliant. In [14], a startup voltage of 35-mV is reached but a mechanical switch is needed to start up, which increases the cost. As shown before, the proposed circuit offers high reliability under no load, full load, and overload conditions. Compared with [13] and [14], the proposed system needs a higher input voltage. A minimum of 40 mV or higher is needed for the circuit to work properly, while this value is 20 and 25 mV for [13] and [14], respectively. More detailed information can be found in Table II.

VI. Conclusion

A complete energy harvesting power supply for implantable pacemakers has been proposed in this paper. A TEG provides the input voltage for the circuit from the temperature difference found between the body and the ambience. Using the FBB technique, a low-voltage oscillator and a low-voltage CP have been designed and simulated which enable the circuit to start up from input voltages as low as 60 mV. Applying a 40-mV input voltage, the output voltage of the proposed power supply is 2.5 V under any load conditions. The circuit includes an internal reference voltage. No extra reference voltage source is needed. The maximum deliverable power to the load is 130 μW. The circuit was designed in such a way that overload conditions are tolerated. The HSPICE simulation results prove the effectiveness of the proposed circuit.

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