COEN-4720 Embedded Systems

Lecture 3
Introduction to ARM Cortex-M0+ Processor

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BE THE DIFFERENCE.

Outline

- Overview of ARM Cortex-M0+ processor
- STM32L053R8 MCU (microcontroller unit)

Cortex-M0+ Processor

- Released in 2012
- RISC general purpose 32-bit microprocessor
- Most energy-efficient Arm processor available for embedded applications
- Part of Cortex-M family of processors, which is for the mainstream microcontroller market
- Short pipeline
  - Two stage - Cortex-M0+ processor
  - Three stages - Cortex-M0, Cortex-M3, Cortex-M4 processors
  - Six stage - Cortex-M7 processor

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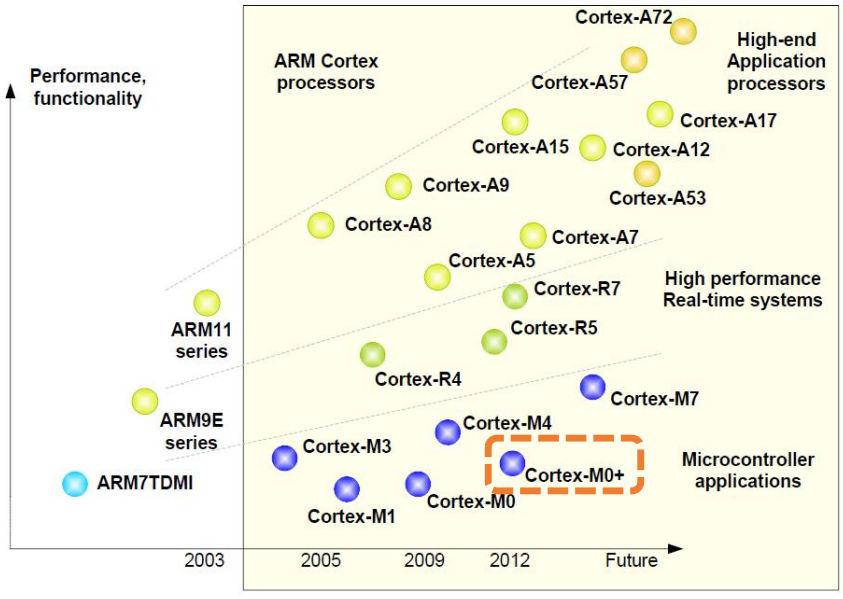

Figure 1.3
Overview of the ARM processor family.

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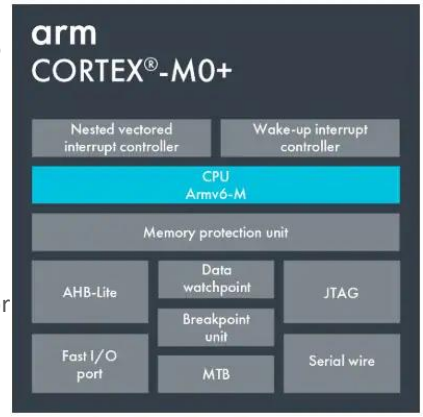
Cortex-M0+ Processor: Key Features

- Armv6-M architecture
- Bus interface AHB-lite, Von Neumann bus architecture with optional single cycle I/O interface
- Thumb/Thumb-2 subset instruction support (56 instructions, mostly 16 bit)
- 2-stages pipeline
- Optional 8 regions MPU (mem protection unit) with sub-regions and background region
- Non-maskable interrupt + 1 to 32 physical interrupts
- Wakeup interrupt controller
- Hardware single-cycle (32x32) multiply
- Several sleep modes, with integrated Wait For Interrupt (WFI) a Wait for Event (WFE) plus sleep on exit capability, sleep and deep sleep signals
- JTAG and Serial Wire Debug ports with up to 4 breakpoints and 2 watchpoints
- Optional Micro Trace Buffer



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Instruction Support

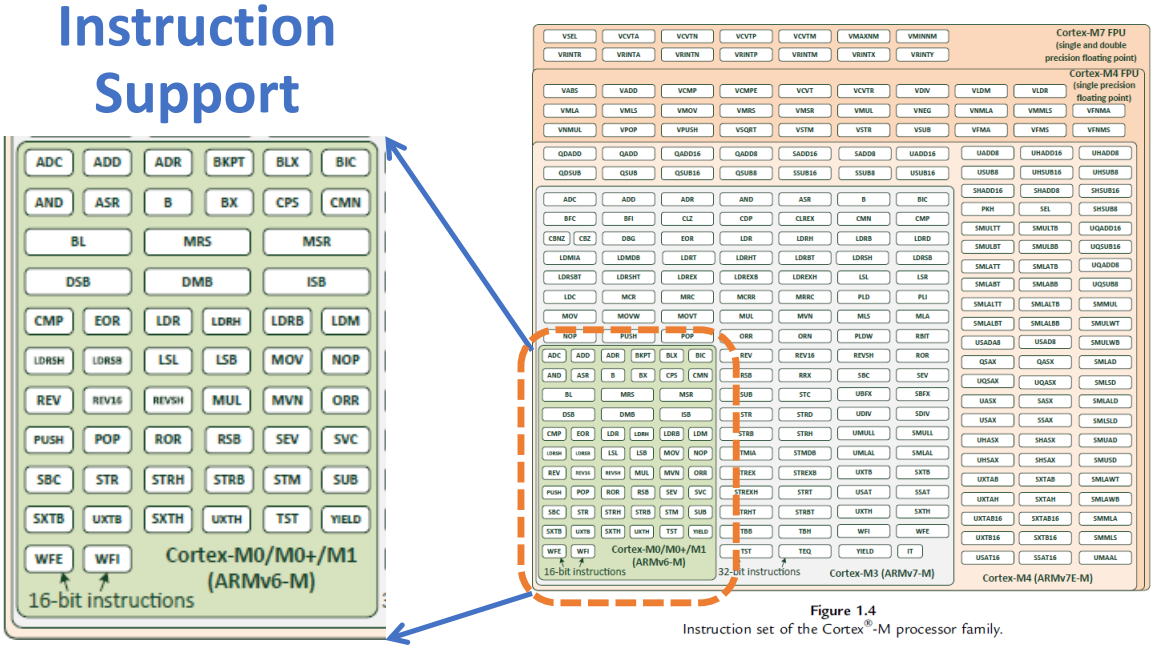

Figure 1.4
Instruction set of the Cortex®-M processor family.

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Two-stage Pipeline

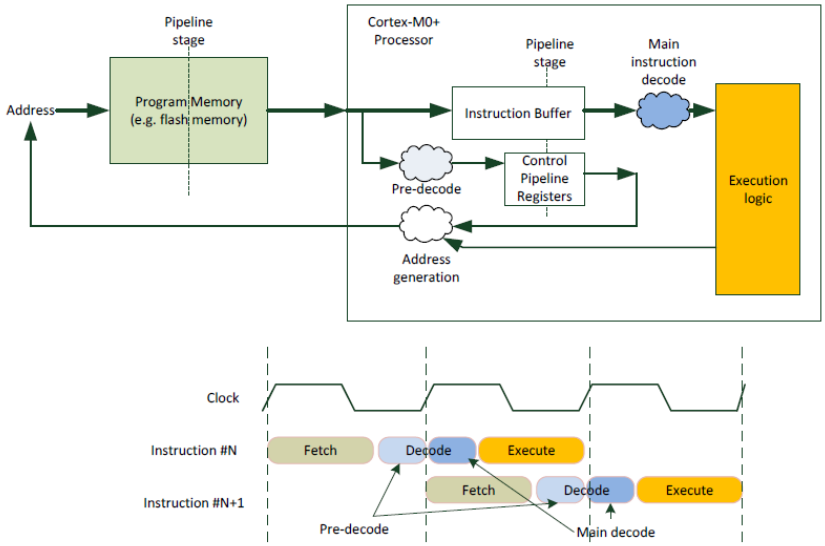

Figure 1.5
Two-stage Pipeline in the ARM® Cortex®-M0+ Processor.

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Table 1.3: An overview of the system level and debug features for various Cortex®-M Processors

Features	Cortex-M0	Cortex-M0+	Cortex-M1	Cortex-M3	Cortex-M4	Cortex-M7
Number of interrupts	1–32	1–32	1, 8, 16, 32	1–240	1–240	1–240
Interrupt priority levels	4	4	4	8–256	8–256	8–256
FPU	-	-	-	-	Optional (single precision)	Optional (single precision/single + double precision)
OS support	Y	Y	Optional	Y	Y	Y
Memory Protection unit	-	Optional	-	Optional	Optional	Optional
Cache	-	-	-	-	-	Optional
Debug	Optional	Optional	Optional	Optional	Optional	Yes
Instruction trace	-	Optional MTB	-	Optional ETM	Optional ETM	Optional ETM
Other trace	-	-	-	Optional	Optional	Optional

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Simplified Cortex-M0+ Block Diagram

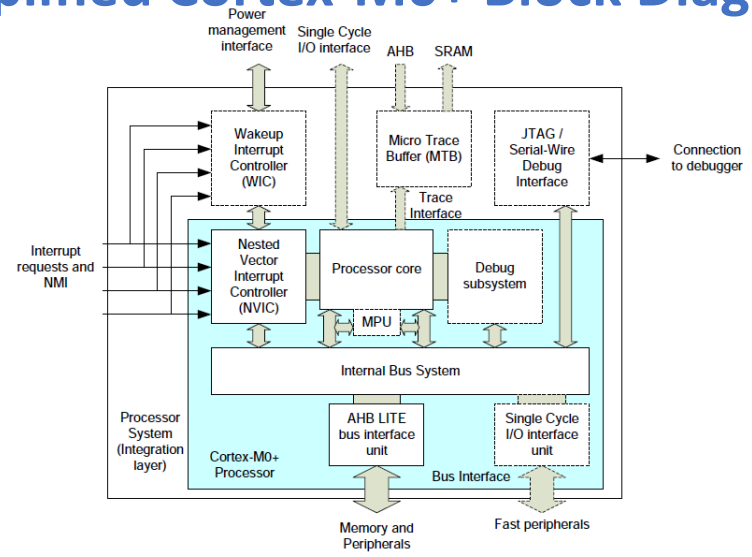

Figure 2.3
A simplified block diagram of the Cortex®-M0+ processor.

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Cortex-M0+ Processor: Memory Addressing

- 32-bit addressing supporting up to 4 GB of memory space.
- The system bus interface is based on an on-chip bus protocol called AHB-Lite, supporting 8-bit, 16-bit, and 32-bit data transfers.
- The AHB-Lite protocol is pipelined, support high operation frequency for the system.
- Peripherals can be connected to a simpler bus based on APB protocol (Advanced Peripheral Bus) via an AHB to APB bus bridge.
- Cortex-M0+ *processor* does not contain memories and peripherals (microcontroller chip designers need to add such components to their MCU designs).

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Example of MCU that uses Cortex-M0+ Processor

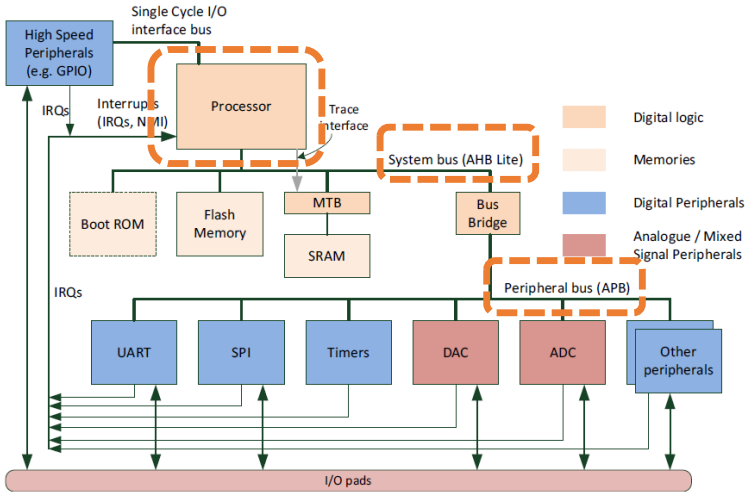

Figure 2.5
A simple system with the Cortex®-M0+ Processor.

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Added Components

- A memory for program code storage, usually a Read-Only-Memory (ROM) component, or reprogrammable memory technologies such as flash memory.
- A read-write memory for data (including variables, stack, etc.), usually based on Static Random Access Memory (SRAM).
- Various types of peripherals.
- High speed peripherals.
- Bus infrastructure components for joining the processor to all the memories and peripherals.

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Cortex-M Processors

- Cortex-M processors use a load/store architecture with three basic types of instructions
  1. **Register-to-register** operations for processing data
  2. **Memory operations** which move data between memory and registers
  3. **Control flow** operations enabling programming language control flow such as if and while statements and procedure calls

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Processor "Register Set"

- 16 user-visible registers
  - R0 to R15
  - All processing takes place in these registers
- Three of these registers have dedicated functions
  - R15 is the Program Counter (PC) - holds the address of the next instruction to execute
  - R14 is a register called Link Register (LR) - holds the address from which the current procedure was called
  - R13 is the Stack Pointer (SP) - holds the address of the current stack top

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Registers

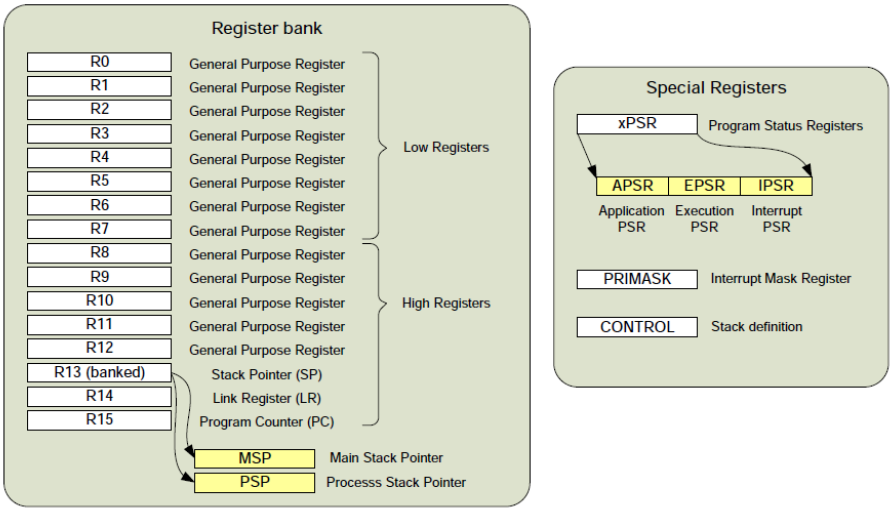

Figure 4.3
Registers in the Cortex®-M0 and Cortex-M0+ processors.

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Cortex-M0+ Processor: Memory Map

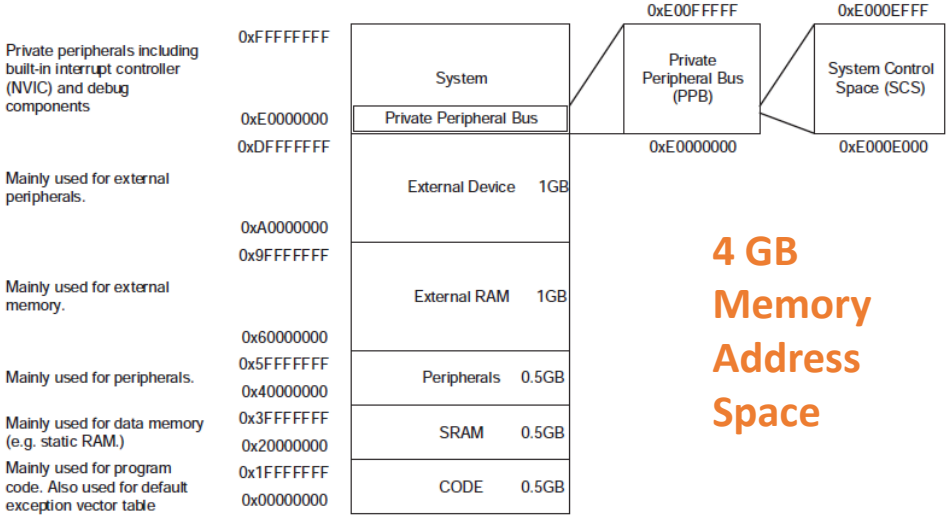

Figure 4.10
Memory map.

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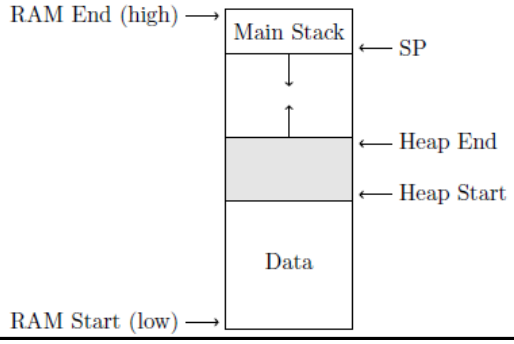
A Note on Program Memory Model

- RAM for an executing program (in systems w/o OS) is divided into three regions
  1. Data in RAM are allocated during the link process and initialized by startup code at reset
  2. The (optional) heap is managed at runtime by library code implementing functions such as **malloc** and **free** which are part of the standard C library
  3. The stack is managed at runtime by compiler generated code which generates per-procedure-call stack frames containing local variables and saved registers



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Application Development: Polling vs. Interrupt Driven

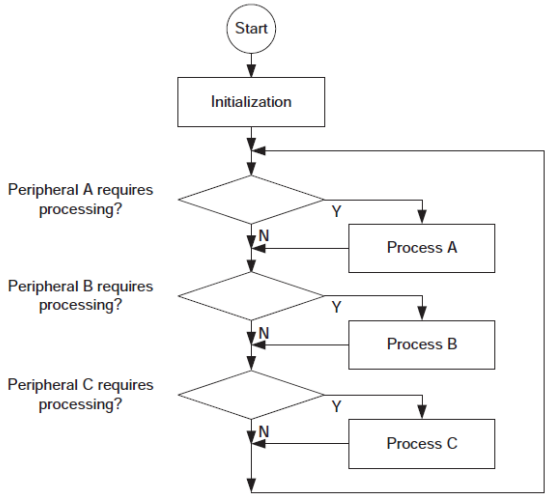

Figure 3.3
Polling method for simple application processing.

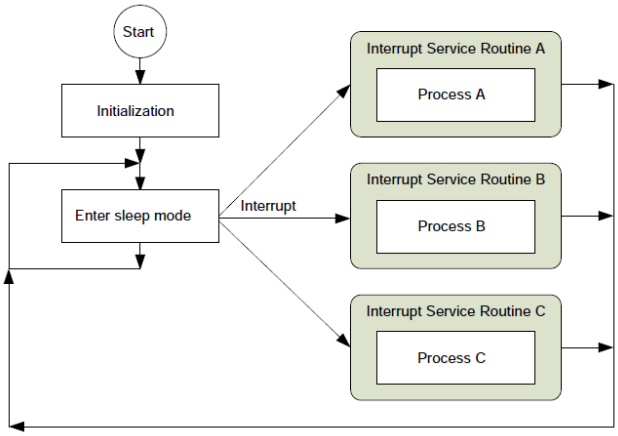

Figure 3.4
Interrupt-driven application.

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Nested Vector Interrupt Controller (NVIC)

- To prioritize interrupt requests and handle other exceptions, Cortex-M processors have a built-in interrupt controller called NVIC.
- Interrupt management function is controlled by several programmable registers in the NVIC.
  - Including the System Timer (SysTick) that provides a regular timer interrupt.
  - Provision for a built-in timer across the Cortex-M family has significant advantage of making OS code highly portable – all OS need at least one core timer for time-slicing.
- These registers are memory mapped, with addresses located within System Control Space (SCS).
- NVIC supports a number of features:
  - Flexible interrupt management
  - Nested interrupt support
  - Vectored exception entry
  - Interrupt masking

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Outline

- Overview of ARM Cortex-M0+ processor
- STM32L053R8 MCU (microcontroller unit)

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Typical MCU Block Diagram

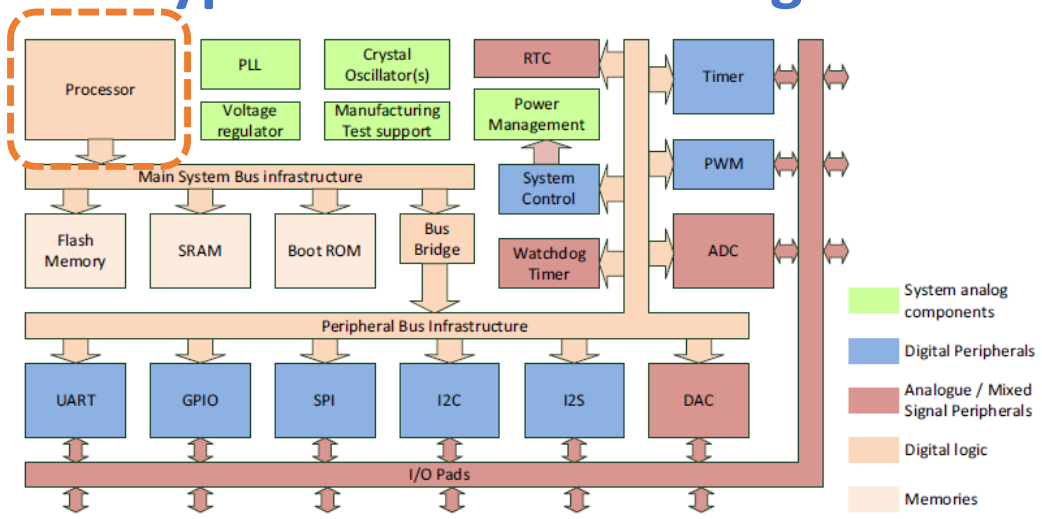

Figure 1.9
A simple microcontroller.

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Typical Peripherals (aka Devices or Components)

Table 1.5: Typical components in a microcontroller

Item	Descriptions
ROM	Read Only Memory—Nonvolatile memory storage for program code.
Flash memory	A special type of ROM, which can be reprogrammed many times, typically for storing program code.
SRAM	Static Random Access Memory—for data storage (volatile)
PLL	Phase Lock Loop—a device to generate programmable clock frequency based on a reference clock.
RTC	Real Time Clock—a low power timer for counting seconds (typically runs on a low power oscillator), and in some cases also for minutes, hours and calendar functions.
GPIO	General Purpose Input/Output—a peripheral with parallel data interface to control external devices and to read back external signals status.
UART	Universal Asynchronous Receiver/Transmitter—a peripheral to handle data transfers in a simple serial data protocol.
I2C	Inter-Integrated Circuit—a peripheral to handle data transfers in a serial data protocol. Unlike UART, a clock signal is required and can provide higher data rate.
SPI	Serial Peripheral Interface—another serial communication interface for off-chip peripherals.
I2S	Inter-IC Sound—a serial data communication interface specifically for audio information.
PWM	Pulse Width Modulator—a peripheral to output waveform with programmable duty cycle.
ADC	Analog to Digital Converter—a peripheral to convert analog signal-level information into digital form.
DAC	Digital to Analog Converter—a peripheral to convert data values into analog signal level.
Watchdog timer	A programmable timer device for ensuring the processor is running program. When enabled, the program running needs to update the watchdog timer within a certain time gap. If the program crashed, the watchdog timed out and this can be used to trigger a reset or a critical interrupt event.

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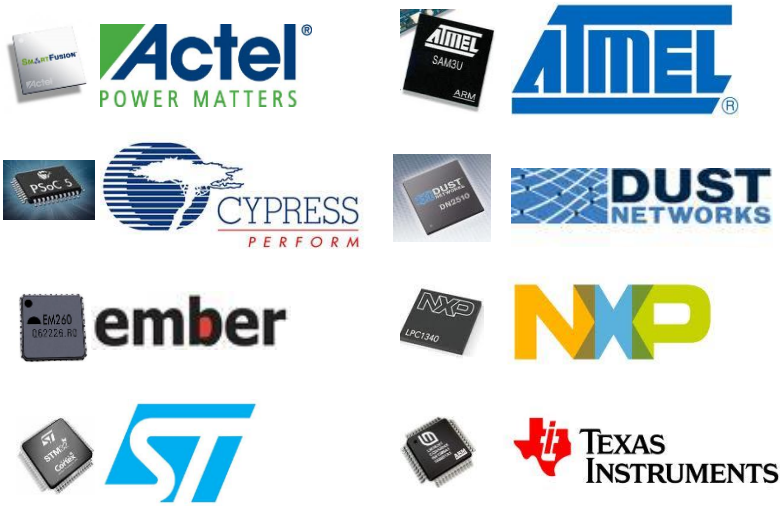
- While there is significant overlap between MCU families and their peripherals, there are also important differences.
- Laboratory of this course: focus on **STM32L053R8** MCU.



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STM32L053R8 - Datasheet

life.augmented

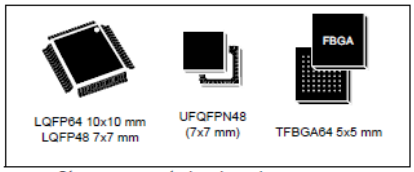
STM32L053C6 STM32L053C8
STM32L053R6 STM32L053R8

Ultra-low-power 32-bit MCU Arm®-based Cortex®-M0+, up to 64KB Flash, 8KB SRAM, 2KB EEPROM, LCD, USB, ADC, DAC

Datasheet - production data

Features

- Ultra-low-power platform
  - 1.65 V to 3.6 V power supply
  - -40 to 125 °C temperature range
  - 0.27 µA Standby mode (2 wakeup pins)
  - 0.4 µA Stop mode (16 wakeup lines)
  - 0.8 µA Stop mode + RTC + 8-Kbyte RAM retention
  - 88 µA/MHz in Run mode
  - 3.5 µs wakeup time (from RAM)
  - 5 µs wakeup time (from Flash memory)
- Core: Arm® 32-bit Cortex®-M0+ with MPU
  - From 32 kHz up to 32 MHz max.
  - 0.95 DMIPS/MHz
- Memories
  - Up to 64-Kbyte Flash memory with ECC
  - 8-Kbyte RAM
  - 2 Kbytes of data EEPROM with ECC
  - 20-byte backup register
  - Sector protection against R/W operation



  - Step-up converted on board
- Rich Analog peripherals
  - 12-bit ADC 1.14 Msps up to 16 channels (down to 1.65 V)
  - 12-bit 1 channel DAC with output buffers (down to 1.8 V)
  - 2x ultra-low-power comparators (window mode and wake up capability, down to 1.65 V)
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- 7-channel DMA controller, supporting ADC, SPI, I2C, USART, DAC, Timers
- 8x peripheral communication interfaces

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STM32L053R8 - Datasheet

- Up to 51 fast I/Os (45 I/Os 5V tolerant)
- Reset and supply management
  - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
  - Ultra-low-power POR/PDR
  - Programmable voltage detector (PVD)
- Clock sources
  - 1 to 25 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - High speed internal 16 MHz factory-trimmed RC (+/- 1%)
  - Internal low-power 37 kHz RC
  - Internal multispeed low-power 65 kHz to 4.2 MHz RC
  - PLL for CPU clock
- Pre-programmed bootloader
  - USART, SPI supported
- Development support
  - Serial wire debug supported
- LCD driver for up to 8×28segments
  - Support contrast adjustment
  - Support blinking mode
  - 1x USB 2.0 crystal-less, battery charging detection and LPM
  - 2x USART (ISO 7816, IrDA), 1x UART (low power)
  - Up to 4x SPI 16 Mbits/s
  - 2x I2C (SMBus/PMBus)
- 9x timers: 1x 16-bit with up to 4 channels, 2x 16-bit with up to 2 channels, 1x 16-bit ultra-low-power timer, 1x SysTick, 1x RTC, 1x 16-bit basic for DAC, and 2x watchdogs (independent/window)
- CRC calculation unit, 96-bit unique ID
- True RNG and firewall protection
- All packages are ECOPACK2

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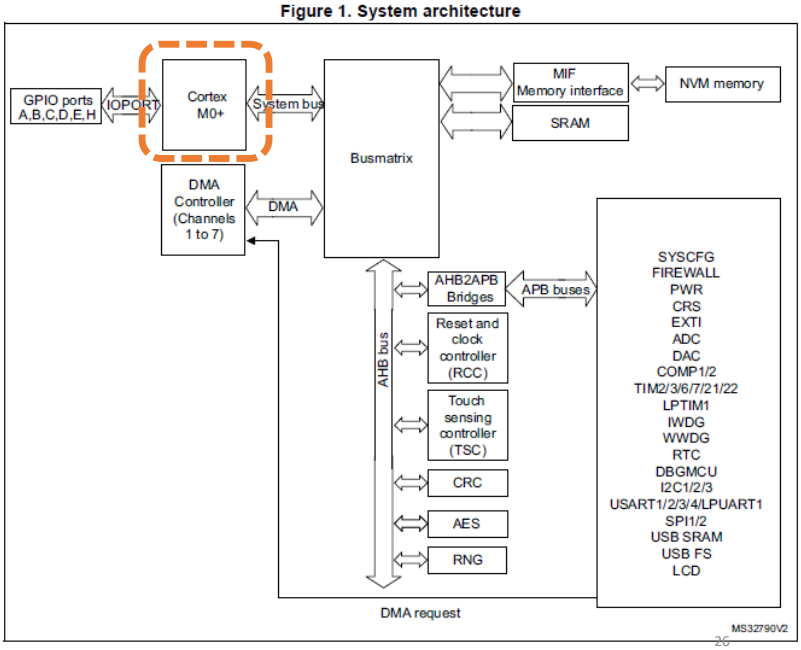
STM32L053R8 – Reference Manual

Note: See Datasheet for a more detailed, large diagram.

Figure 1. System architecture



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Main System

- Two masters:
  - Cortex-M0+ core (AHB-lite bus)
  - GP-DMA (general-purpose DMA)
- Three slaves:
  - Internal SRAM
  - Internal Non-volatile memory
  - AHB to APB, which connects all the APB peripherals
- These are interconnected using a multilayer AHB bus architecture

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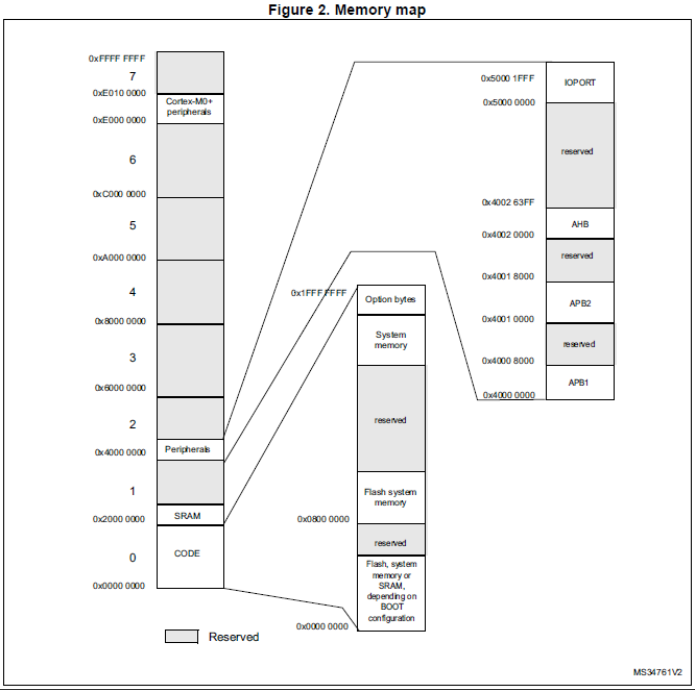
MCU Memory Map

Figure 2. Memory map



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Low Power Modes

- Support dynamic voltage scaling (DVS) to optimize power consumption in Run mode. There are three power consumption ranges:
  - Range 1 (VDD range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
  - Range 2 (full VDD range), with a maximum CPU frequency of 16 MHz
  - Range 3 (full VDD range), with a maximum CPU frequency limited to 4.2 MHz
- Seven low-power modes:
  1. Sleep mode
  2. Low-power run mode
  3. Low-power sleep mode
  4. Stop mode with RTC
  5. Stop mode without RTC
  6. Standby mode with RTC
  7. Standby mode without RTC

Note: See page 14 of Datasheet for detailed information on these power modes.

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MCU Development Board: NUCLEO-L053R8

Figure 1. STM32 Nucleo-64 board

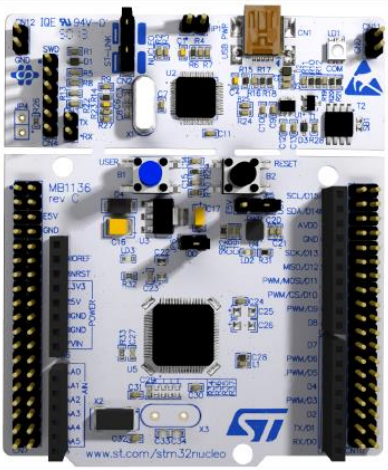
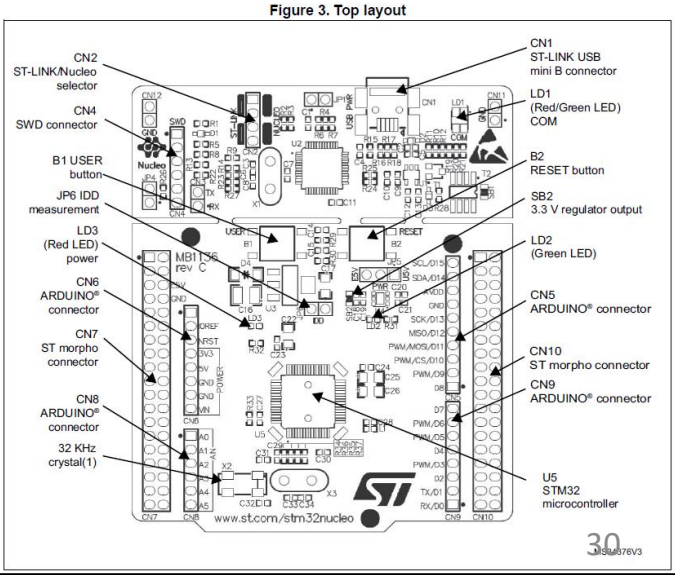


Figure 3. Top layout



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Board Features

The STM32 Nucleo board offers the following features:

- STM32 microcontroller in LQFP64 package
- Three LEDs:
  - USB communication (LD1), user LED (LD2), power LED (LD3)
- Two push-buttons: USER and RESET
- Two types of extension resources
  - ARDUINO® Uno V3 connectivity
  - ST morpho extension pin headers for full access to all STM32 I/Os
- Flexible board power supply:
  - USB VBUS or external source (3.3 V, 5 V, 7-12 V)
  - Power management access point
- On-board ST-LINK/V2-1 debugger and programmer with SWD connector
  - Selection-mode switch using the kit as a standalone ST-LINK/V2-1
- USB re-enumeration capability. Three different interfaces supported on USB:
  - Virtual COM port
  - Mass storage
  - Debug port
- Comprehensive free software libraries and examples available with the STM32Cube MCU Package
- Arm® Mbed™(a) (see http://mbed.org)

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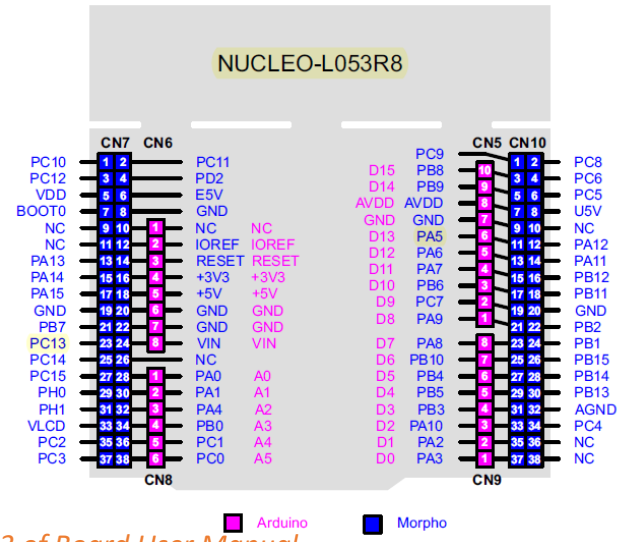
NUCLEO-L053R8 Pinout



Note: See page 33 of Board User Manual

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References & Credits

- [Book 2] Joseph Jiu, *The Definitive guide to ARM Cortex-M0 and Cortex-M0+ Processors*, 2015.
- Arm® Cortex®-M0+ in a nutshell
  - https://www.st.com/content/st_com/en/arm-32-bit-microcontrollers/arm-cortex-m0-plus.html
- STM32L053R8 MCU
  - Datasheet
  - User Manual
- NUCLEO-L053R8 Board
  - User Manual

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