Probabilistic Aspects of Crosstalk Problems in CMOS ICs*

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Abstract - *In this paper we present a probabilistic approach for analyzing the dependence of crosstalk effects on input pattern correlations. In particular, we show that the effects of coupling between interconnections, in current VLSI ICs, are strongly dependent on the spatio-temporal correlations at the primary inputs. Consequently, a smaller fraction of the total number of nets poses true crosstalk problems and only that fraction should be considered at lower levels of abstraction. The analysis is carried out at the logic-level of abstraction, which provides efficient CPU run time and memory usage.*

Keywords: *crosstalk, input pattern correlations, non-critical pairs, probabilistic analysis.*

I. INTRODUCTION

As a consequence of aggressive scaling of nowadays CMOS devices toward deep submicron dimensions, the crosstalk (CT) has become an important issue that needs to be addressed. Its effects are becoming increasingly problematic as coupling capacitances increase at a greater rate compared to the ground capacitances of the interconnections with lateral scaling. Consequently, the coupling capacitances can contribute with as much as 75% to the interconnect delay. Process technology options (such as Cu/low-k wires), device sizing, repeaters, asymmetric pitches and scaling of thickness are common methods to deal with CT problems [1].

The fact that the crosstalk is indeed a serious concern in designing VLSI circuits is evident from a relatively rich literature which can be roughly divided as follows (see Fig. 1):

1. ***Modeling & Estimation of CT.*** These approaches are low-level methods, mainly at transistor-level. All of them consider essentially the interaction between two nets denoted as *victim* and *aggressor*. These methods are concerned especially with crosstalk modeling, providing formulae for estimating the magnitude and shape of the voltage induced in the victim net. Some of these techniques work in time domain supplying exact or approximate formulae for the total coupled noise voltage [2], [3]. Others attack the subject in the frequency domain, benefitting from some simplification or reduction of the mathematical model, but finally they still provide time formulae. These expressions are numerical models for alternative simulation relative to Spice simulations, trading-off accuracy vs. CPU time and memory usage.
2. ***Crosstalk discarding/reduction.*** This category comprises techniques that are closer to the level of the local routing. They assume a given layout, which is corrected by doing local re-routing until all the crosstalk problems are resolved [6], [7], [9].
3. ***Crosstalk avoidance***. This category comprises techniques where the existence of noise is captured in constraints under which the following steps at lower levels of abstraction (global routing) are conducted [4].

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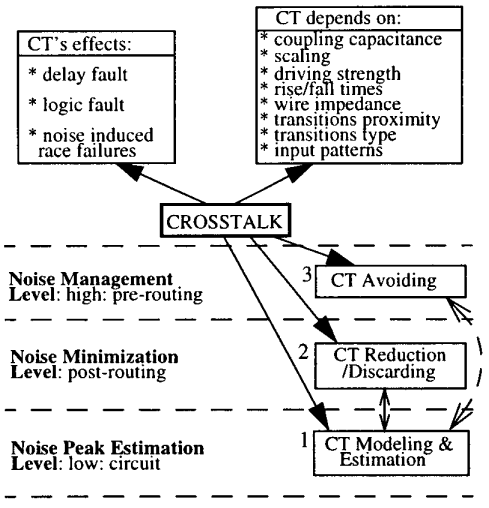

Fig.1. Crosstalk issues

As it is shown in Fig. 1, the last two categories are interdependent with the first one, in the sense that they can use some formulae given by methods in the first category. We also note that, while in the first two categories there is a sizeable body of research, the third direction is far less explored. With a very few exceptions (which handle crosstalk at higher levels of abstraction using information from the physical layout), the advantages of approaching CT issues at high levels are practically overlooked.

In this paper, we explore this very third option and try to provide new insights. Our work aims at finding the set of interconnection pairs which *will not pose* crosstalk problems during normal operation of the circuit. Capturing input pattern dependencies models the effect of the environment upon the structure of the target circuit, in particular its layout, that is designed to work under certain conditions which are assumed to be known to the designer. This modeling can result (e.g. by using a CT-aware router) in a simpler circuit (realized on a smaller area) compared to the case when the circuit is designed without taking into account the input pattern correlations. Consequently, our research tries to *complement* the existing CT approaches and offer a new perspective on these issues. Its novelty consists of:

- proposing a probabilistic crosstalk analysis framework, at logic-level of abstraction, while taking into account the effect of *input pattern correlations*;
- showing that the *input pattern correlations* may significantly influence the actual percentage of *non-critical interconnection pairs*.

It should be also noted that our approach (also the one in [4]) does not provide an exact solution. However, it can significantly reduce the search space during subsequent design steps (in

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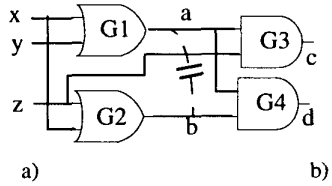
particular routing) and then provide important time and area savings.

The paper is organized as follows: in Section II we illustrate the intuition behind our work. Section III formalizes, at circuit level, the probabilistic analysis. In Section IV, we give some experimental results and point out further work. Finally, we conclude by summarizing our main contribution.

II. MOTIVATION

To illustrate the effect of input patterns correlations on the operation of the target circuit, let us consider the simple example in Fig. 2.a. Let us suppose that nodes ***a*** and ***b*** are coupled through some coupling capacitance as shown in the figure.



a) b)

S1-count			S2-pseudo		
xyz	ab	cd	xyz	ab	cd
000	00	00	001	01	00
001	01	00	100	11	01
010	10	00	110	11	01
011	11	11	111	11	11
100	11	01	011	11	11
101	11	11	101	11	11
110	11	01	010	10	00
111	11	11	000	00	00

Fig. 2: Example circuit

Assume now that this circuit is fed successively by two input sequences S1 and S2. S1 is an exhaustive sequence generated by a 3-bit counter, while S2 is a pseudorandom (PR) sequence generated with a maximal-length linear feed-back shift register (LFSR) modified to include the all-zero pattern. The circuit is simulated with HSpice. Analyzing the simulation results we can make the following observations:

a) Sequence S1 (see Fig. 4.a). In this case, there is a moment (t=50ns) when ***a*** swings upward (0→1) while ***b*** swings downward (1→0). These transitions can cause a *delay fault* consisting in a delay change of both G3 and G4 gates. In spite of this favorable situation, *the delay fault is not "seen"* at the output of G3. Indeed, this is because the other input of G3 receives the signal z which cannot be 1 since otherwise ***b*** could not have a transition (1→0). However, we note that the *delay fault is "seen"* at the output ***d***, which presents a glitch.

This phenomenon was exploited in [4]; it is clearly a consequence of the structural/functional properties of the circuit. It was observed in [4] that if, for instance, node ***a*** had all its transitions 1→0 (0→1) within the ODC of ***a***, then this node should not be considered as being a *critical node*. However, if the circuit has a configuration where several levels exist between ***a*** and ***c*** (as shown in Fig. 3), then even though the *delay fault* is not seen at ***c***, a *glitch* can emerge at the outputs of intermediate gates; this can cause additional problems and extra power dissipation.

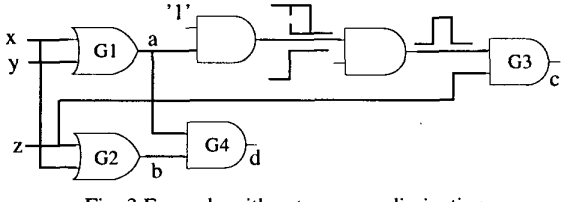


Fig. 3 Example with extra power dissipation

Continuing our analysis of the waveforms, we see that at t=25ns, when ***b*** swings upward (0→1) and ***a*** is 0, the effect of the coupling capacitance is a significant peak (*logic fault*) at ***a***. However this logic fault is not seen at the output ***c***. This is because G3 has at one of its inputs the signal z switching from 1 to 0.

In summary, the pair ***(a, b)*** *will pose* CT problems when the circuit is fed with *sequence S1*.

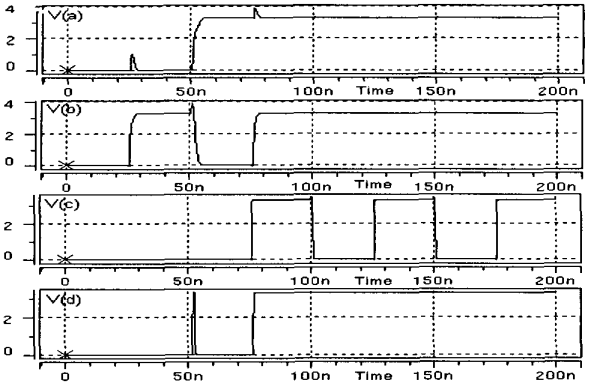


Fig. 4.a: Waveforms obtained for the counted sequence (S1)

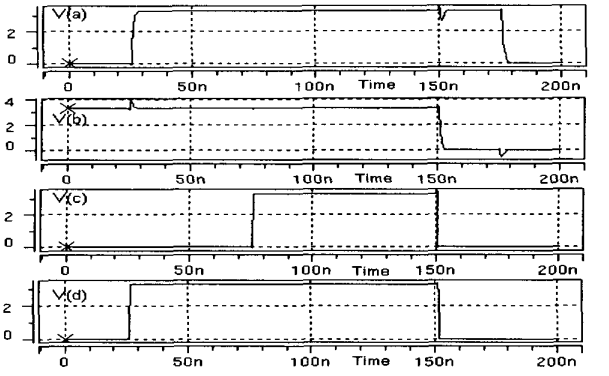


Fig. 4.b: Waveforms obtained for the PR sequence (S2)

b) Sequence S2 (see Fig. 4.b). In this case, there is no condition favorable to the emergence of a *delay fault*. Instead, there is a situation when a *logic fault* can occur (t=150ns). When ***b*** swings downward (1→0) and ***a*** is 1, the effect of coupling capacitance gives a significant peak (*logic fault*) at ***a***. However, the output of G3 *does not see* that logic fault since G3 has, at the other input, the signal z switching from 1 to 0.

We may conclude that the pair ***(a, b)*** *will not pose* CT problems when the circuit is fed with *sequence S2*.

From this simple example, we can see that during normal operation, some input patterns can pose CT problems (due to some coupled interconnects) while others cannot. In general, for every type of input pattern correlations, the *critical nodes set* and *critical interconnection pairs set* (the *non-critical interconnection pairs set* as well) will be different, offering more or less freedom during subsequent steps in the design flow. To account for (and benefit) from the dependence of the number of non-critical pairs set on input pattern correlations, a probabilistic technique is presented in the next section.

III. PROBLEM FORMULATION

3.1 Notations

In what follows, the *PO* will denotes the set of primary outputs and *INT* the set of all internal nodes. Also, *DLNS* will be used for the *non-critical pairs set* from a delay/logic faults point of view with *x* as *victim* and *y* as *aggressor* (*D*elay/*L*ogic *N*on-Critical Pairs *S*et).

Let $p(x_{i\to j}, y_{p\to q})$ be the transition probabilities of the signal x from i to j *and* the signal y from p to q (that is, the probability of the event "x switches from i to j and y from p to q, simultaneously"). Also, let $p(x_{i\to j}, y_{p\to q}, f_{u\to v})$ denote the transition probabilities of the signal x from i to j and the signal y from p to q and the signal f from u to v (that is, the probability of the event "x switches from i to j and y from p to q and f from u to v, simultaneously").

3.2 The proposed approach

To formally define our approach, we first discuss the *causes* and *effects* of the CT. The effects of the CT between two coupled interconnects (*victim* and *aggressor*) are threefold:

a. ***Delay fault***. This type of fault affects the gate delay which, in turn, can change *the critical path delay* and *glitches*. It emerges when signals of the two coupled interconnections undergo *opposite swings*.

b. ***Logic fault***. In this case the voltage induced in the victim interconnect by the aggressor interconnect is *greater* than a threshold which determines the circuit to malfunction, viz. a logic *error* emerges when the risk tolerance bound is exceeded.

c. ***Noise-induced race failures***. As observed in [8], this type of fault is a consequence of the *delay fault*. It emerges when a *hold-time is violated* in pipelined circuits.

We must distinguish between ***delay fault*** and ***logic fault***, as well as between their ***causes*** and ***effects***. Thus, considering a fault-free circuit and the same circuit but with x and y coupled by crosstalk (that is, there is a coupling capacitance C_c between x and y which determines the circuit malfunctioning because of a *delay/ logic fault* emergence), we consider the following two conditions:

1. *Fault favorable transitions shall not exist* between two nodes for certain input pattern correlations during circuit's normal operation. These *favorable transitions* are schematically shown in Fig. 5, where *opposite swinging fronts*, 0→1 and 1→0 (e.g. first line in the table) mean *delay faulty transitions,* while transitions 0→0, 0→1 (e.g. third line in the table) mean *logic faulty transitions*. Thus, if a coupling capacitance exists between x and y, then it will not be a concern since there are no favorable conditions when a fault can emerge.

2. *Fault favorable transitions may exist*, but *"the effect"* of a *delay/logic fault*, which can emerge due to a possible CT between x and y, *shall not be seen* at any of the primary outputs of the circuit.

	x y $i\to j$ $p\to q$	
α	0 1 1 0 1 0 0 1	delay fault
	0 0 0 1 1 1 1 0	logic fault (x as *victim*, y as *aggressor*)

Fig. 5 'Faulty' delay/logic situations

Based on the above two conditions the computation of the *non-critical pair set* is made as follows:

1. Given $x, y \in INT$, if

$$\alpha = jp\bar{q} + \bar{j}\bar{p}q = 1$$
$$p(x_{i\to j}, y_{p\to q}) < \varepsilon \qquad (1)$$

and $fanout(x) \geq fanout(y)$, then $DLNS = DLNS \cup \{(x, y)\}$.

In this case, if x as victim and y as aggressor are coupled together, there will emerge neither *delay fault* in x or y, nor *logic fault* in x as *victim*. This is because α captures both situations when a *delay fault favorable condition* may exist, as well as any *favorable condition for a logic fault* in x due to y.

The transition probabilities in (1) are computed only for those cases when α=1; that is, the four situations given in Fig. 5. Thus, they shall be better called the probabilities of the event "(x switches from 0 to 1 and y switches from 1 to 0) OR (x switches from 1 to 0 and y switches from 0 to 1) OR (x switches from 0 to 0 and y switches from 0 to 1) OR (x switches from 1 to 1 and y switches from 1 to 0) simultaneously".

2. Given $x, y \in INT$, if $\forall f \in PO$

$$\beta = (jp\bar{q} + \bar{j}\bar{p}q)(\overline{u \oplus v}) = 1$$
$$p(x_{i\to j}, y_{p\to q}, f_{u\to v}) > \varepsilon \qquad (2)$$

and $fanout(x) \geq fanout(y)$, then $DLNS = DLNS \cup \{(x, y)\}$.

In this case, if x as victim and y as aggressor are coupled together, their CT interaction (manifested as a *delay fault* in x or y, or *logic fault* in x) is *not seen* at any primary output. It should be noted that this case represents a stronger condition than the property exploited in [4]. In this case, the β parameter makes the probability from relation (2) be called the probability of the event "{(x switches from 0 to 1 and y switches from 1 to 0) OR (x switches from 1 to 0 and y switches from 0 to 1) OR (x switches from 0 to 0 and y switches from 0 to 1) OR (x switches from 1 to 1 and y switches from 1 to 0)} AND {(f switches from 0 to 0) OR (f switches from 1 to 1)} simultaneously". We also note that the significance of ε in (1) is *"significantly small"*, while the one of ε in (2) is *"significantly large"*.

IV. RESULTS

To asses the validity of the approach, two types of experiments are performed: one, involving circuits fed with three different types of sequences which have different input pattern correlations (namely *counted*, *pseudorandom*, and *Gray-coded* sequences) and other one, involving circuits fed with *pseudorandom* and *highly correlated* sequences (the last ones being taken from real applications).

a) Counted, pseudorandom and Gray-coded sequences

To compute the estimates of ***the non-critical pairs percentages***, the probabilities in (1) and (2) are calculated for every pair of internal interconnections (x, y), for each circuit. These probabilities are directly computed using the simulation results from SIS. .

Table 1: Isolated non-critical pairs percentages

Seq. Length	Circuit	No. Inputs/ Outputs	No. Nodes	Counted	Pseudo-Random	Gray-code
32	majority	5/1	8	19.64%	25.00%	25.00%
32	xor5	5/1	9	0.00%	5.55%	0.00%
16	cm42a	4/10	12	9.04%	4.54%	12.12%
16	circ	4/3	13	21.79%	12.72%	8.82%
32	cm82a	5/3	17	8.08%	3.67%	8.82%
64	con1	7/6	20	23.94%	1.57%	40.78%
32	rd53	5/3	22	7.14%	8.87%	6.06%
2048	cm85a	11/3	29	44.33%	3.44%	40.47%
4096	cm151a	12/2	30	14.59%	0.45%	20.91%
16384	cu	14/11	31	42.68%	1.82%	61.93%
256	misex1	8/7	41	7.62%	2.25%	9.14%
16384	14/5	43	43	37.09%	1.43%	46.17%
512	ldd	9/19	62	20.01%	3.83%	22.68%
128	z4ml	7/4	89	3.17%	0.54%	3.23%
256	f51m	8/8	95	13.99%	0.87%	15.37%

Table 1 shows the results obtained for some combinational benchmarks. The measurements are given as *percentages of non-critical pairs* so they can be related to the results given in [4]. It can be seen that, for most of the circuits, the isolated percentage of non-critical pairs varies significantly with the *type* of input patterns. For instance, in the case of the benchmark *con1*, the *isolated percentage of non-critical pairs* is 23.94% for the counted sequence, 1.57% for the pseudorandom sequence, and 40.78% for the Gray-coded sequence.

b) Pseudorandom and highly correlated sequences

In this case the circuits are fed at the primary inputs with sequences presenting two different kind of input pattern correlations: the first category is a *pseudorandom sequence* generated with a maximal-length linear feed-back shift register (LFSR), while the other one is a *highly correlated sequence* obtained from real applications. Table 2 shows the results obtained in the same manner as in the first set of experiments.

Table 2: Isolated non-critical pairs percentages

Seq. Length	Circuit	No. Inputs/ Outputs	No. Nodes	Pseudo-Random	Highly Correlated
4000	unreg	36/16	86	0.50%	18.85%
4000	b9	41/21	91	0.30%	7.27%
4000	9symml	9/1	144	3.91%	27.95%
4000	ttt2	24/21	146	3.40%	13.84%
4000	mul4	16/8	181	0.14%	1.13%
4000	C432	36/7	199	0.46%	6.96%
4000	C1355	41/32	260	12.39%	10.87%
4000	C499	41/32	299	12.31%	12.60%
4000	C1908	33/25	359	16.35%	15.73%

It can be seen again a high variation; for instance, in the case of 9symml benchmark, for a sequence of 4000 vectors, *the isolated percentage of non-critical pairs* is 3.9% for the pseudorandom sequence, while for the highly correlated sequence it becomes as large as 27.95%.

To verify that none of the non-critical pairs found by the probabilistic approach is in fact a critical one, we devised the following strategy and applied it to a few simple circuits:

Step 1: *Layout* the circuits using Mentor Graphics tools.

Step 2: Do *extraction* to obtain the HSpice netlist file including all the coupling capacitances between interconnections.

Step 3: *Simulate* these circuits with HSpice and visually analyze all the waveforms at the internal nodes (in order to count interconnection pairs between which coupling effects appear as glitches). These pairs are denoted as *critical interconnection* pairs.

Step 4: *Compare* HSpice results with those obtained with our probabilistic analysis. If any *critical pair* found with HSpice is not among those predicted as being *non-critical* within probabilistic analysis, we conclude that the set of non-critical pairs obtained by means of the probabilistic analysis is correct.

In Table 3 we present some results obtained using the above strategy. This table shows the number of pairs posing crosstalk problems for the chosen circuits for three different sequences with very different correlation types. It should be noted that the outputs are excluded (although they may pose crosstalk problems too). None of them, found as posing CT problems with HSpice, is among those declared by our probabilistic approach as being non-critical pairs.

Table 3: Number of pairs found as posing crosstalk problems

Circuit	Counted Seq.	Pseudo-Random Seq.	Gray Seq.	Total possible pairs
circ	5	5	1	156
C17	2	1	0	12
con1	6	7	3	462

We remark that, for most of the circuits, the isolated percentage of non-critical pairs varies significantly with the type of input sequences. However, for some circuits, the difference is insignificant (e.g. C499, C1908 in Table 2). This is because these circuits have many outputs but it may be also related to the internal functionality of the circuits. It should be noted, however, that the *non-critical pairs* (even in the case with similar percentages for the same circuit) *may not be the same* when the circuits are fed with different types of sequences with different types of input pattern correlations. In the case when the circuits are fed with the pseudorandom sequence the results are slightly different from those reported in [4].

To analyze larger benchmark circuits, we plan to use the formulae reported in [5] for probabilities computation. In this case, the simulation with SIS is not needed anymore. In fact, this represents one of the targeted advantages: to perform the probabilistic analysis at a level of abstraction as high as possible. This way, input spatio-temporal correlations are captured, CPU time is very short, and a CT-aware-routing becomes possible due to a significant shrunk of the search space. We also have to mention that, by using formulae from [5], some accuracy will be lost compared to the case of using explicit simulation. As future work, we also plan to extend this approach to sequential circuits where the percentage of isolation is expected to be even higher.

V. CONCLUSION

In this paper, we have shown that input pattern correlations can dramatically influence the number of interconnection pairs between which real crosstalk coupling problems may exist. A probabilistic approach has been proposed aiming at determining, at the logic-level of abstraction, the set of non-critical interconnection pairs. This way a CT-aware-routing becomes possible and then significant area/time savings may result.

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