Distributed Minimum Energy Point Tracking for Systems-on-Chip

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***Abstract*—We propose a new design approach for systems-on-chip. The goal of the proposed design approach is to minimize the overall energy consumption dynamically, during runtime. The proposed approach builds on the well known globally asynchronous locally synchronous design style. To minimize power noise and losses, we propose to use a single high-voltage global power delivery network. Locally integrated DC-DC regulators generate a discrete range of supply voltage levels. These regulators are dynamically controlled by novel minimum energy point tracking (MEPT) controllers. The goal of the MEPT controllers is to seek in a decentralized fashion the minimum energy consumption point of each voltage frequency island via dynamic voltage and frequency scaling, thereby driving the entire SoC toward minimum energy consumption. Since the proposed MEPT controller relies on the extremum-seeking control theory, its stability is theoretically guaranteed. While the scope of this project is to address all design aspects of the proposed design style, in this paper, our contribution is to introduce and discuss the MEPT controller. Simulation results demonstrate its operation.**

***Index Terms*—system-on-chip; power consumption; minimum energy point tracking;**

I. Introduction

Thanks to downscaling, it is projected that future systems-on-chip (SoCs) will integrate hundreds or more cores on the same chip. While this will enable the implementation of multiple concurrent applications on the SoC platform, several design challenges are exacerbated by the increase in chip area and device density. Global interconnects have higher delay which negatively affects the performance. Clock distribution has become more challenging due to the increased clock skew and jitter. Power consumption has increased beyond acceptable limits. High power consumption results in on-chip thermal and reliability problems. In addition, larger process variations increase the uncertainty of signal delays and result in variability of circuit delay and power. Finally, workload variations contribute to varying on-chip temperatures.

One promising design approach to address many of the above problems is the voltage and frequency islands (VFIs) design style [1]–[3]. The idea is to partition the SoC into several islands. Then, these islands can be supplied independently with different supply voltages and clock frequencies in ways that reduce power consumption while meeting system performance constraints. A simplified representation of this design approach is shown in Fig.1. Note that because there is no global clock signal and each island operates at its own clock frequency, this design style is an effective realization of the globally asynchronous locally synchronous (GALS) design philosophy. To ensure synchronization of the communication between different VF islands, mixed-clock mixed-voltage FIFO queues must be utilized as shown in Fig.1. Applications can be mapped on this hardware platform such that energy consumption is minimized while system performance meets the desired target. Moreover, dynamic voltage and frequency scaling (DVFS) can be utilized to further optimize power and thermal profiles during runtime.

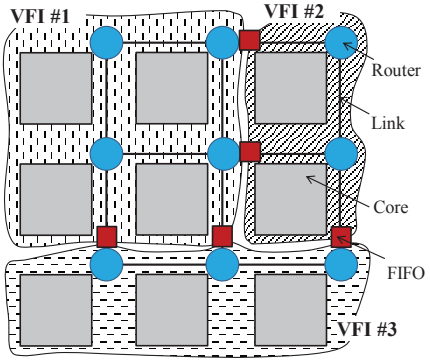

Fig. 1. Illustration of the voltage frequency island design approach: a network-on-chip based chip multiprocessor is partitioned into three voltage frequency islands (VFIs). The finest VFI partitioning is when each core represents a VF island.

In this paper, we present a design approach for SoCs that builds on the VFI approach. The primary goal is to dynamically minimize the overall energy consumption of the SoC. This is achieved by utilizing DVFS to control each VF island to operate at its minimum energy point (MEP).

II. Related Work and Contribution

Minimizing energy consumption, especially for battery powered systems, has always been a key focus in integrated circuit and embedded systems design. Dynamic voltage and frequency scaling (DVFS) has been a very popular technique that was used to implement dynamic thermal and power management techniques [4]. Within the context of voltage frequency islands (VFI) design style, DVFS can be utilized to adapt the power/energy consumption of a system to dynamically react to workload variations [5]. Aside from providing a framework to develop DVFS techniques, voltage islanding

has been investigated also as a mechanism to cope with the problem of process variations in [6].

A simpler form of DVFS is to employ only dynamic voltage scaling (DVS) [7]. A DVS system operates the circuit at the minimum voltage that meets the required performance, thereby achieving savings in power consumption. Moreover, in subthreshold circuits, the voltage can be further lowered to operate at the minimum energy point (MEP) during periods of low activity [8], [9]. By dynamically tracking the MEP, additional reductions in power consumption can be achieved as demonstrated in [10], [11]. Limitations of previous MEP tracking solutions include the fact that they do not guarantee the stability of their control techniques. In addition, previous tracking algorithms require a microcontroller, and the DC-DC conversion is done by utilizing off-chip inductors [10].

We propose a new design style for SoCs that builds on VF islanding, distributed DC-DC converters, and DVFS to provide a holistic approach for addressing the aforementioned limitations and problems. We propose to generate supply voltages and clock signals locally for each VF island. The generation of different supply voltages is done by the integrated DC-DC converters controlled in a *decentralized* fashion by intelligent minimum energy point tracking (MEPT) controllers. Since the proposed MEPT controller is developed using the extremum-seeking control theory, its stability is theoretically guaranteed. In addition, because each VF island is locally controlled during runtime, its minimum energy consumption point is individually tracked irrespective of the adverse impact of process, voltage and temperature (PVT), aging, and workload variations. In this paper, our main contribution is to introduce and discuss the proposed MEPT controller.

III. Minimum Energy Point

It is well known that at circuit level, there is a minimum energy point (MEP) of operation where the energy consumption of a circuit is minimized. As such, there have been significant research efforts to model the MEP and to develop solutions to drive the circuit operation toward it. Previous work focused primarily on the energy-delay product (EDP). However, it has been shown that the power-delay product (PDP) offers a better tradeoff between energy and delay than energy-delay or power-energy products (PEP), especially for submicron technologies [12]. Therefore, in this paper, we build our discussion around PDP. However, the proposed design style can be readily applied to work with EDP or PEP figures of merit too.

For example, a typical power-delay product (PDP) variation for a VF island or computational core is shown in Fig.2. Note that in general due to process, voltage, and temperature (PVT) variations these curves will not be identical for different hardware realizations of the same core. Moreover, these curves can also be influenced by temperature variations and by the activity of the core, which may not be known at design time [13]. In general, the *uncertainty* of the PDP curve and of the location of its minimum energy point (MEP) can be described as the corridor area depicted with hashed lines in Fig.2. It is precisely the task of the MEPT circuit proposed in this paper to seek the optimal operating point (minimum energy consumption, V_{DDM} in Fig.2) of each VF island or core. Since each VF island or core has its MEP tracked by its own MEPT controller, the entire SoC has its overall energy consumption driven in a distributed fashion toward a minimal value.

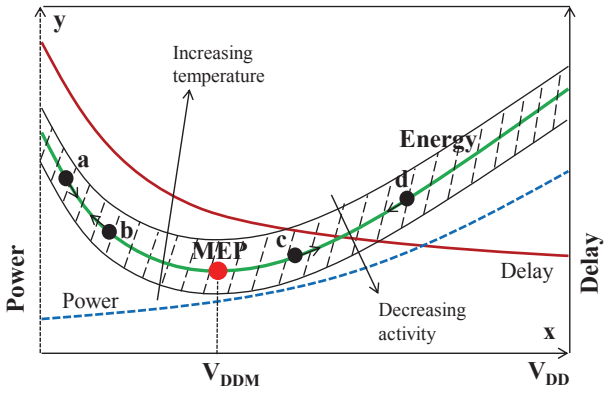

Fig. 2. Typical variation of the power-delay product (PDP) as a function of the supply voltage V_{DD} for a VF island or core. Voltage V_{DDM} corresponds to the minimum energy point. Points *a,b,c,d* represent illustrative cases of extremum-seeking mechanism discussed later.

Note that the MEPT controller tracks the MEP point irrespective of the differences between different realizations of the same VF island or core. Therefore, a nice characteristic of the proposed design approach is that the MEP tracking is immune to PVT and workload variations.

IV. Proposed Minimum Energy Point Tracking System

The proposed VFI based design approach is described in the block diagram from Fig.3. The main components of this diagram include the MEPT controller, the DC-DC converter, the ring oscillator, a current sensor, and enhanced flip-flops. The MEPT controller computes the power delay product (PDP) of the modified VF island and controls the DC-DC converter (which in turn controls the ring oscillator) to drive the operation of the VF island toward the minimum energy point. To attain the MEP, the integrated DC-DC converter is appropriately controlled to switch the supply voltage of the VF island to lower or higher levels. At the same time, the frequency levels are also adjusted with the help of the ring oscillator. The adjustment of the frequency and voltage levels is done in specific order. When the frequency is adjusted from high to low, it is scaled down before the voltage is decreased. When the frequency is adjusted from low to high, the voltage is increased before the frequency is scaled up.

The *load* in the diagram shown in Fig.3 is represented by the modified VF island or core whose minimum energy point is sought. The modification consists of the utilization of enhanced flip-flops. These enhanced flip-flops enable the measurement of the delay of the most critical timing paths in the VF island. They are similar to the flip-flops studied in [14], [15] and continuously monitor the circuit delay and

its variation. This delay information together with information on voltage and absorbed current are utilized as input into the proposed MEPT controller, which is discussed in the next section.

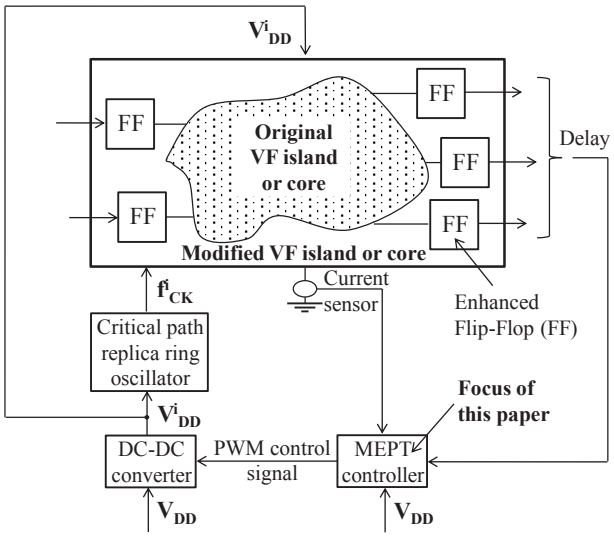

Fig. 3. System level block diagram of the proposed minimum energy point tracking system. This system is applied to each voltage frequency island from Fig.1.

The main characteristics and potential benefits of the proposed design approach illustrated in Fig.3 include: 1) The MEPT controller continuously monitors the operation of the target VF island and dynamically controls its voltage and frequency such that the MEP is attained. The MEP is attained regardless of the magnitude of PVT variations for the given *circuit instance*. 2) Since circuit delay degradation (possibly due to aging or PVT variations) is also monitored via the enhanced flip-flops, frequency throttling can be utilized to prevent delay faults. 3) Locally integrated DC-DC converters eliminate the need for multiple global power and clock distribution networks and help to reduce power losses. An additional benefit of the integrated DC-DC converters, is that they can help mitigate the problem of IR drop [16].

The proposed hardware platform is very versatile and can be utilized to further investigate DVFS based thermal and power management schemes. In addition, one can also explore software level optimization techniques based on task scheduling and migration in multiprocessor SoCs.

V. MEPT Controller

The block diagram of the proposed minimum energy point tracking (MEPT) controller is shown in Fig.4. Its idea draws from the concept of *maximum* power point tracking, which has been investigated extensively in the power electronics community [17]. The difference is that here our objective is to track the *minimum* energy point along the convex variation of the power-delay product (PDP). The main novelty, compared to previous works on MEP tracking solutions, is that here we develop the MEPT controller using the extremum-seeking control theory [18].

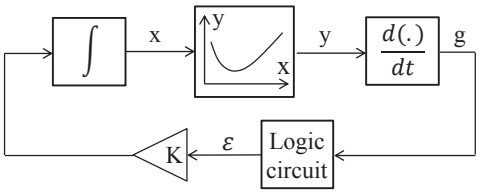

Fig. 4. Block diagram of the extremum-seeking control circuit, MEPT, from Fig.3.

It can be shown (see Appendix A) that the behavior of this system can be described by:

$$\frac{dx}{dt} = -K \cdot sign\left(\frac{dy}{dx}\right) \tag{1}$$

and that the equilibrium point $dx/dt = 0$ is stable. The variables x and y correspond to the supply voltage V_{DD} and the energy consumption in Fig.2.

One of the main advantages of the proposed MEPT controller is that its stability is theoretically guaranteed because it is based on theory of extremum-seeking control. This is not the case with all previous related works.

A. Simulation with Simulink

To verify the correct operation of the MEPT controller, we simulated the block diagram from Fig.4 in Simulink [19]. In our simulations, we use the PDP variation of a computational core similar to that studied in [9]. Simulation results reported in Fig.5 show how the optimum V_{DD} is tracked (shown as arrow $1 \rightarrow 2$) when the system starts from an operation point, 1, located to the right of the MEP. Later in our simulation experiment, we introduce a sudden change of the PDP curve (to mimic for example workload variations). This translates into a sudden jump of the MEP. The MEP jump is easily tracked by the the MEPT controller, which changes V_{DD} to its new optimum point as shown by the arrow $2 \rightarrow 3$ in Fig.5.a.

B. Simulation with Spice simulator

To further investigate the operation of the MEPT controller, we adopt the circuit-level solution studied in [17] and utilize it for our purposes. The schematic diagram of the circuit-level solution is shown in Fig.6, which we simulate using a Spice simulator [20]. Note that, while such simulations are enough to verify the correct operation of the MEPT controller, the actual physical implementation of this circuit is as a complete CMOS integrated solution rather than a discrete component based solution as in [17].

The circuit-level solution requires an analog multiplier, a differentiator, an integrator, and a hysteretic comparator, which are easily identifiable in Fig.6. For the purpose of this discussion, we set the inputs V_x and V_y (which correspond to the *Delay* and *Current sensor* readings from Fig.3) such that their product V_{xy} (which corresponds to y in Fig.4) varies as shown in the top plot of Fig.7. In this case, V_{xy} is varied to mimic movements up and down along the convex curve of y from Fig.4. When this movement is upward, corresponding to

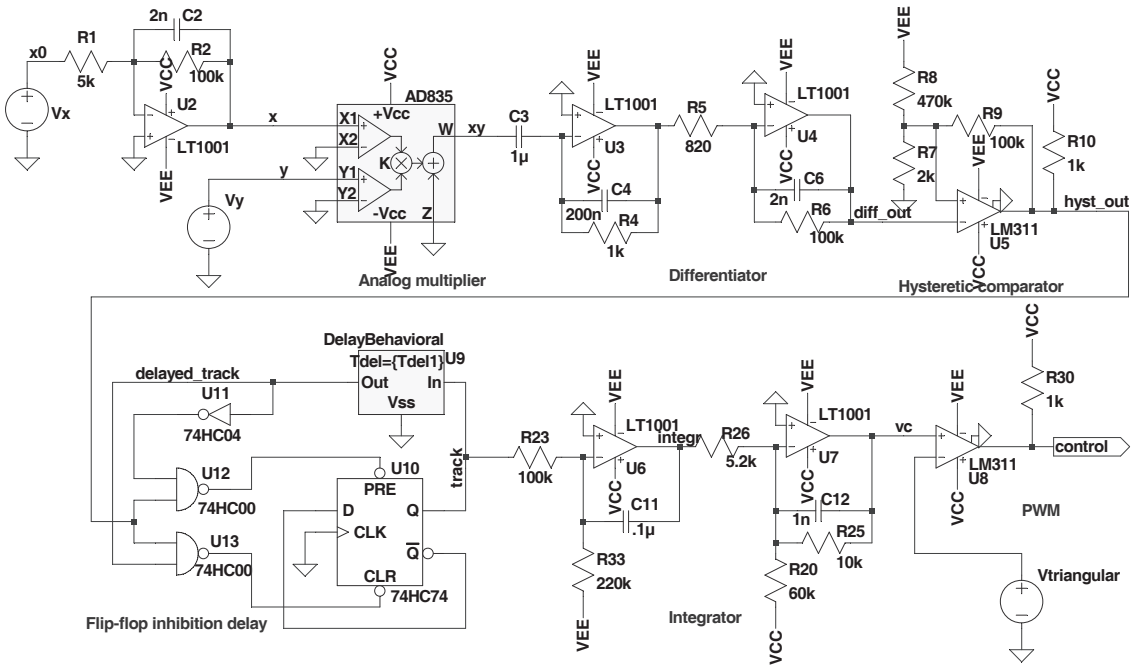

Fig. 6. Schematic diagram of the circuit-level MEPT solution simulated with the Spice simulator.

the first half of the top plot in Fig.7, the PWM control signal shown in the bottom plot of Fig.7 (which is the control signal coming out of the MEPT controller in Fig.3 to control the DC-DC converter) increases its on/off duty cycle. This variation of the PWM control signal is utilized in the block diagram of Fig.3 to switch the supply voltage to a lower level. This discussion is similar for the case when the movement on the curve of y from Fig.4 is downward. This case is captured by the second half of the plots in Fig.4, which also shows the MEPT's internal signals $V(hyst\_out)$ and $V(track)$.

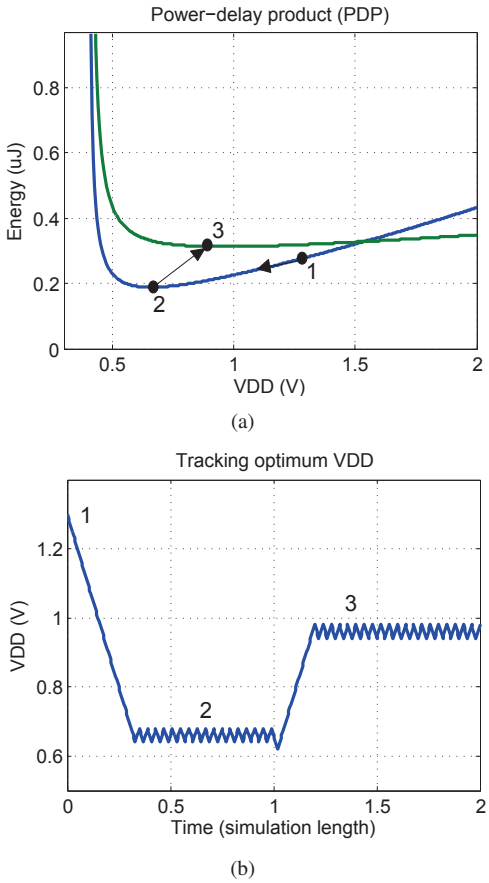

Fig. 5. (a) Power-delay product curves simulated in Simulink. (b) Tracking of optimum V_{DD} for a value of $K = 2$ in Fig.4.

VI. Discussion and Open Problems

Because the design approach proposed in this paper builds on the GALS philosophy, the resulting SoC platform bene-

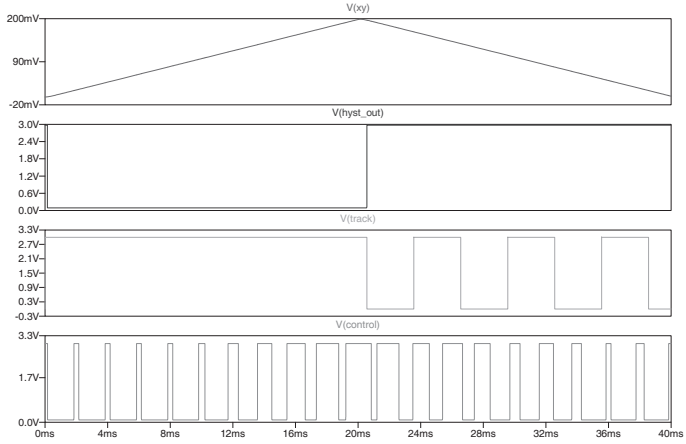

Fig. 7. Spice simulation waveforms for the circuit from Fig.6. The top plot *mimics* the movement up and down on the curve from Fig.4. The bottom plot shows the resulting PWM control signal utilized by the DC-DC converter of Fig.3 to switch between different supply voltage levels.

fits from inherent properties already known for the globally asynchronous design style [21]. These benefits include lower instantaneous maximum power consumption, high operating speed, less emission of electromagnetic noise (local clocks tend to tick at random points in time), robustness towards variations in fabrication process parameters, supply voltage, and temperature, better composability and modularity. In addition, the distributed nature of the MEPT circuits make the proposed SoC architecture scalable.

High-voltage transmission of power across the chip (similar to the transmission systems in electric grids) simplifies the design of the global power network, minimizes losses (due to the smaller currents), and decreases the number of I/O pins. Even though this concept has been discussed/analyzed before [22], [23] and integrated DC-DC converter solutions have been proposed [24]–[27], the overall design and analysis of such an on-chip power transmission and distribution approach is still largely an open problem.

Finally, while the equilibrium point of the system in Fig.2 is guaranteed to be stable (as a direct benefit of the extremum-seeking control theory used to develop the proposed MEPT controller), the stability of the whole system in terms of FIFO queue occupancies is not very clear. To guarantee the stability of the whole system, we may need a global manager that operates as a second top-level controller responsible with regulating voltages and frequencies such that FIFO occupancies remain stable [28]. Such investigations are left for future work.

VII. Conclusion

We introduced a new design approach for SoCs with the primary goal of minimizing the overall energy consumption dynamically, during runtime. The key elements of the proposed design style include global asynchronous operation based on VFI partitioning, single high-voltage on-chip power delivery network with locally integrated DC-DC converters, and distributed minimum energy point tracking (MEPT) controllers that implement decentralized DVFS techniques. Since the proposed MEPT controller is developed based on the extremum-seeking control theory, its stability is theoretically guaranteed. Preliminary simulation results demonstrate the correct operation of the proposed MEPT controller.

Acknowledgment

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Appendix A
Derivation of Equation 1

In this appendix, we sketch the derivation of equation (1). We start from the equations describing the behavior of the block diagram in Fig.4, an integrator, and a derivator.

$$\frac{dx}{dt} = -K\epsilon \tag{2}$$

$$g = \frac{dy}{dt} \tag{3}$$

where $\epsilon = \pm 1$ and K is a constant. The logic circuit block operates according to the following rule:

$$\text{Out of logic circuit } = \begin{cases} \text{change sign of } \epsilon & \text{if } g < 0 \\ \text{keep sign of } \epsilon & \text{if } g > 0 \end{cases} \tag{4}$$

The illustrative cases from Fig.2 can be utilized to describe the behavior of the extremum-seeking algorithm.

1. Vector a describes the case when the movement along the curve is such that x is increasing and y is decreasing. That is $(dx/dt)|_{t^-} > 0$ and $(dy/dt)|_{t^-} < 0$. Because this movement is going toward the minimum energy point from the left hand side, the logic circuit from Fig.4 must maintain or keep the sign of ϵ such that $(dx/dt)|_{t^+} = K$

2. Vector b describes the case when the movement along the curve is such that x is decreasing and y is increasing. That is $(dx/dt)|_{t^-} < 0$ and $(dy/dt)|_{t^-} > 0$. Because this movement is going away from the minimum energy point towards the left, the logic circuit must change the sign of ϵ such that the variation along x becomes positive $(dx/dt)|_{t^+} = K$

3. Similarly, vector c moves away from the minimum energy point with $(dx/dt)|_{t^-} > 0$ and $(dy/dt)|_{t^-} > 0$. Hence, the logic circuit from Fig.4 must change the sign of ϵ such that $(dx/dt)|_{t^+} = -K$

4. Finally, vector d moves toward the minimum energy point with $(dx/dt)|_{t^-} < 0$ and $(dy/dt)|_{t^-} < 0$. Hence, the logic circuit must keep the sign of ϵ such that $(dx/dt)|_{t^+} = -K$

Utilizing the fact that dy/dx can be written as $dy/dx = (dy/dt)/(dx/dt)$, the above four cases can be reduced to:

$$\begin{array}{ll} \frac{dx}{dt}|_{t^+} = K & \text{if } \frac{dy}{dx}|_{t^-} < 0 \\ \frac{dx}{dt}|_{t^+} = -K & \text{if } \frac{dy}{dx}|_{t^-} > 0 \end{array} \tag{5}$$

which in turn can be written in compact form as:

$$\frac{dx}{dt} = -K \cdot sign\left(\frac{dy}{dx}\right) \tag{6}$$

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