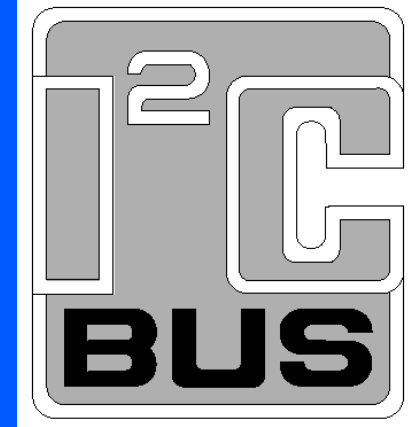


# PHILIPS



## Interface Products Business Line Specialty Logic Product Line I<sup>2</sup>C Logic Family Overview

2Q 2004

Steve Blozis - I<sup>2</sup>C International Product Marketing Manager

Jean-Marc Irazabal – I<sup>2</sup>C Technical Marketing Manager

# Introduction

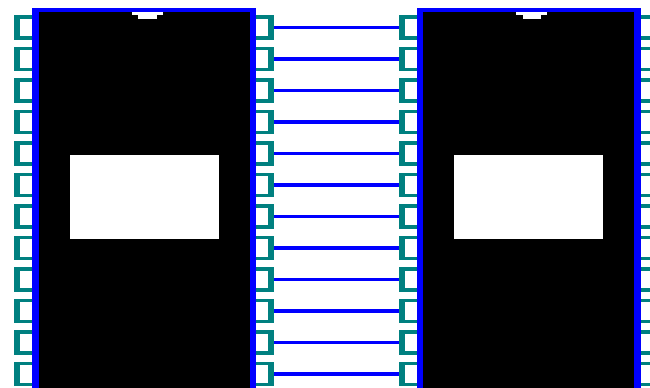
# How the I<sup>2</sup>C Bus Works

The I<sup>2</sup>C (Inter-Integrated Circuit) Bus is a two-wire, low to medium speed, communication bus (a path for electronic signals) developed by Philips Semiconductors in the early 1980s. I<sup>2</sup>C was created to reduce the manufacturing costs of electronic products.

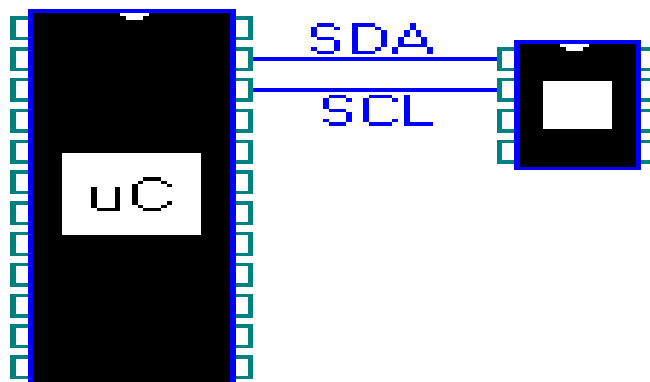
## Low Cost

Prior to I<sup>2</sup>C, chip-to-chip communications used many pins in a parallel interface. Many of these pins were used for inter-chip addressing, selection, control, and data transfers. In a parallel interface, 8 data bits are typically transferred from a sender IC to a receiver IC in a single operation.

I<sup>2</sup>C performs chip-to-chip communications using only two wires in a serial interface, allowing ICs to communicate with fewer pins. The two wires in the I<sup>2</sup>C Bus carry addressing, selection, control, and data, one bit at a time. The Data (SDA) wire carries the data, while the Clock (SCL) wire synchronizes the sender and receiver during the transfer. ICs that use the I<sup>2</sup>C Bus can perform the same function as their larger parallel interface counterparts, but with far fewer pins.

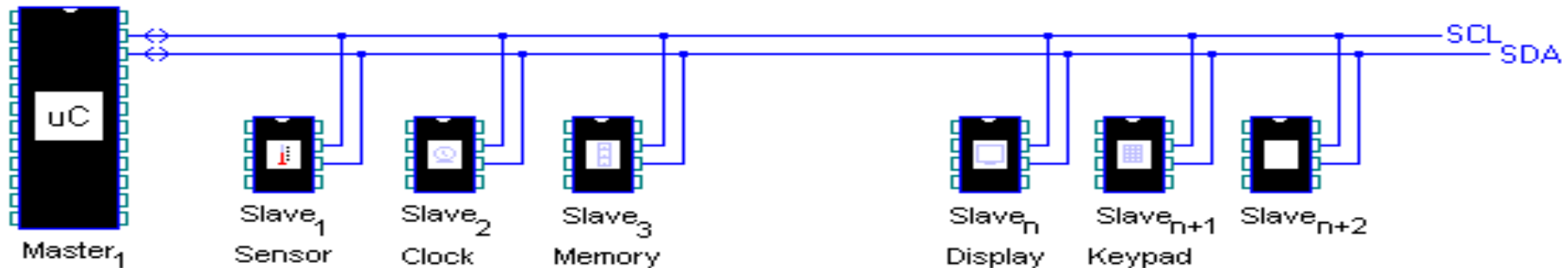


Parallel Interface



I<sup>2</sup>C Serial Interface

# How the I<sup>2</sup>C Bus Works (II)



One I<sup>2</sup>C Master, Multiple Slaves

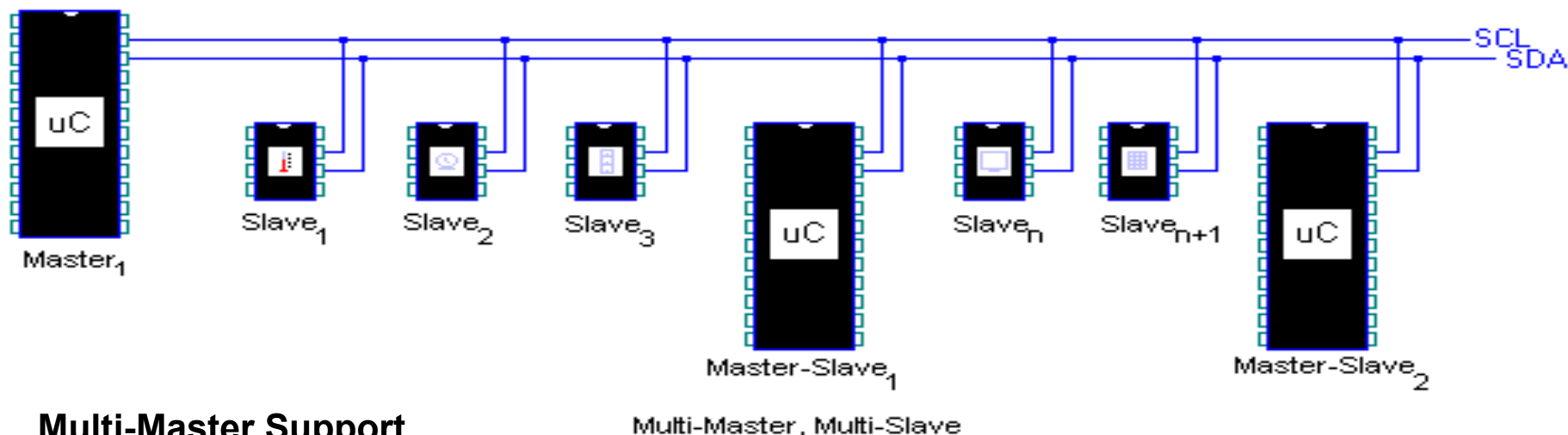
## Master-Slave Hierarchy

I<sup>2</sup>C devices are classified as master or slave. A device that initiates a message is called a master, while a device that responds to a message is called a slave. A device can be master-only, slave-only, or switch between master and slave, as the application requires.

## Multiple Devices

I<sup>2</sup>C can connect many ICs on just two-wires. Each I<sup>2</sup>C slave device has its own unique slave address. When a master sends a message, it includes the slave address at the beginning of the message. All devices on the bus hear the message, but only the slave that recognizes its own address participates in the transfer.

# How the I<sup>2</sup>C Bus Works (III)

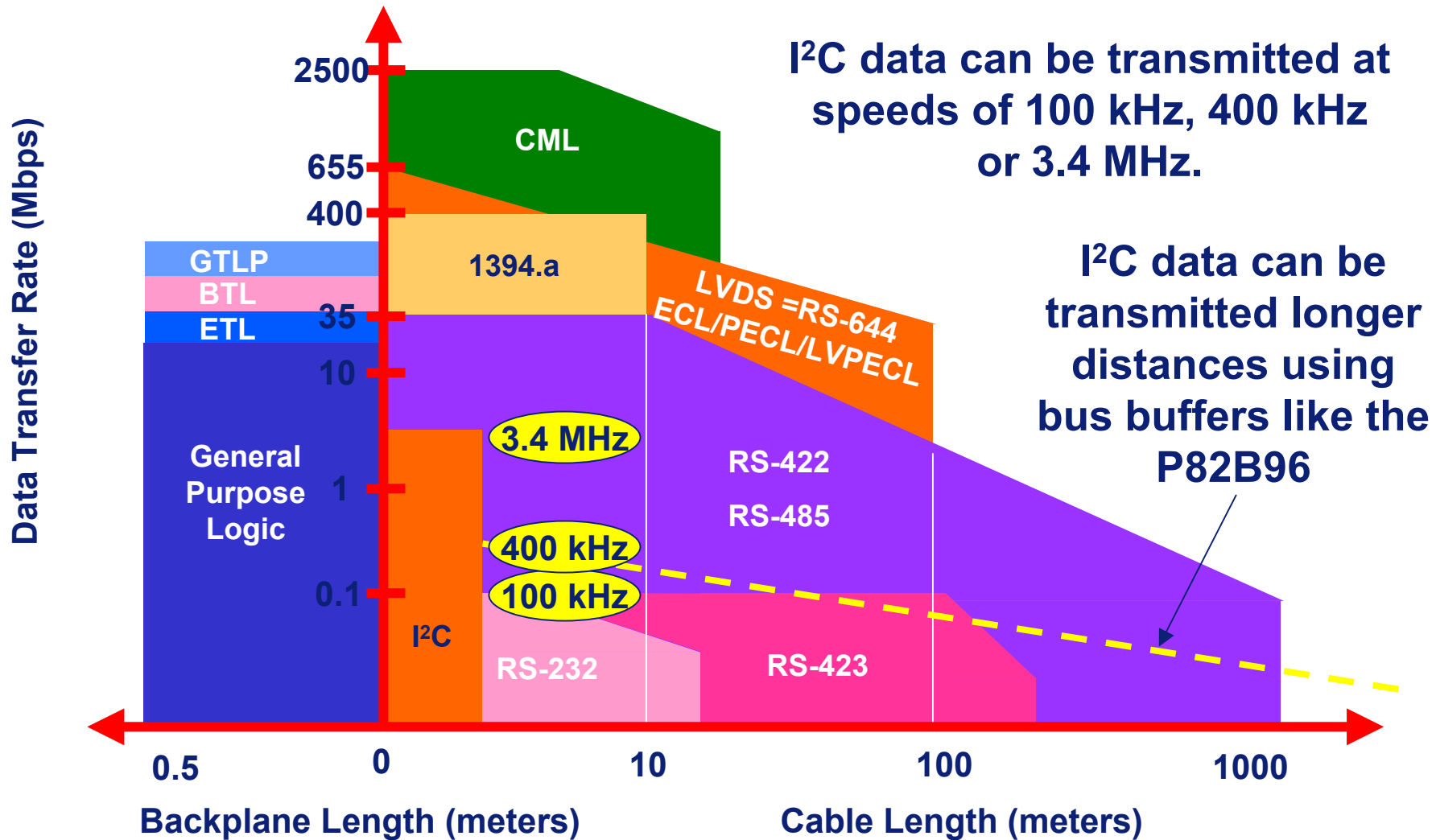


## Multi-Master Support

I<sup>2</sup>C also supports multiple master devices on the bus at the same time, a powerful feature that optimizes bus use by keeping bus message traffic to a minimum. To support multiple masters, I<sup>2</sup>C must resolve signal conflicts, should two or more master devices try to talk on the bus at the same time. This feat, called bus arbitration loss detection, allows a master to detect when its bus signals are conflicting with those of another master. A master that detects arbitration loss terminates its use of the bus, allowing the message generated by another master to cross the bus unharmed.

The I<sup>2</sup>C Bus is a time-proven, industry standard, communication protocol used in a wide variety of electronic products. I<sup>2</sup>C is found in products we use every day, like cellular and conventional telephones, computers, and ATMs (automatic teller machines). Its low cost and powerful features make I<sup>2</sup>C ideal for low to medium speed chip-to-chip communications.

# Transmission Standards

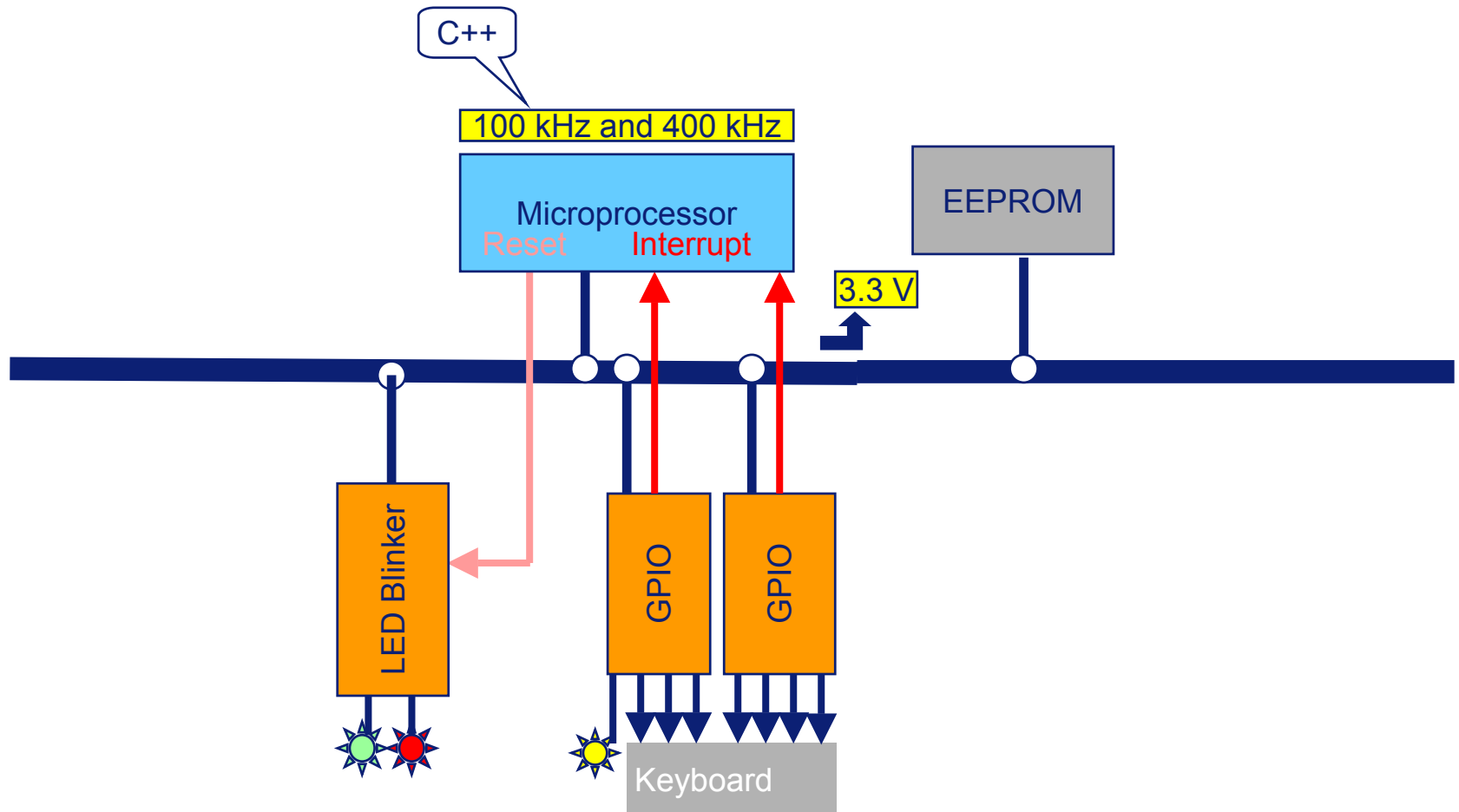


# Typical Applications

- Cell phones
- PDA's
- Lap top computers
- Digital cameras
- Portable test equipment
- Servers
- cPCI and AdvancedTCA

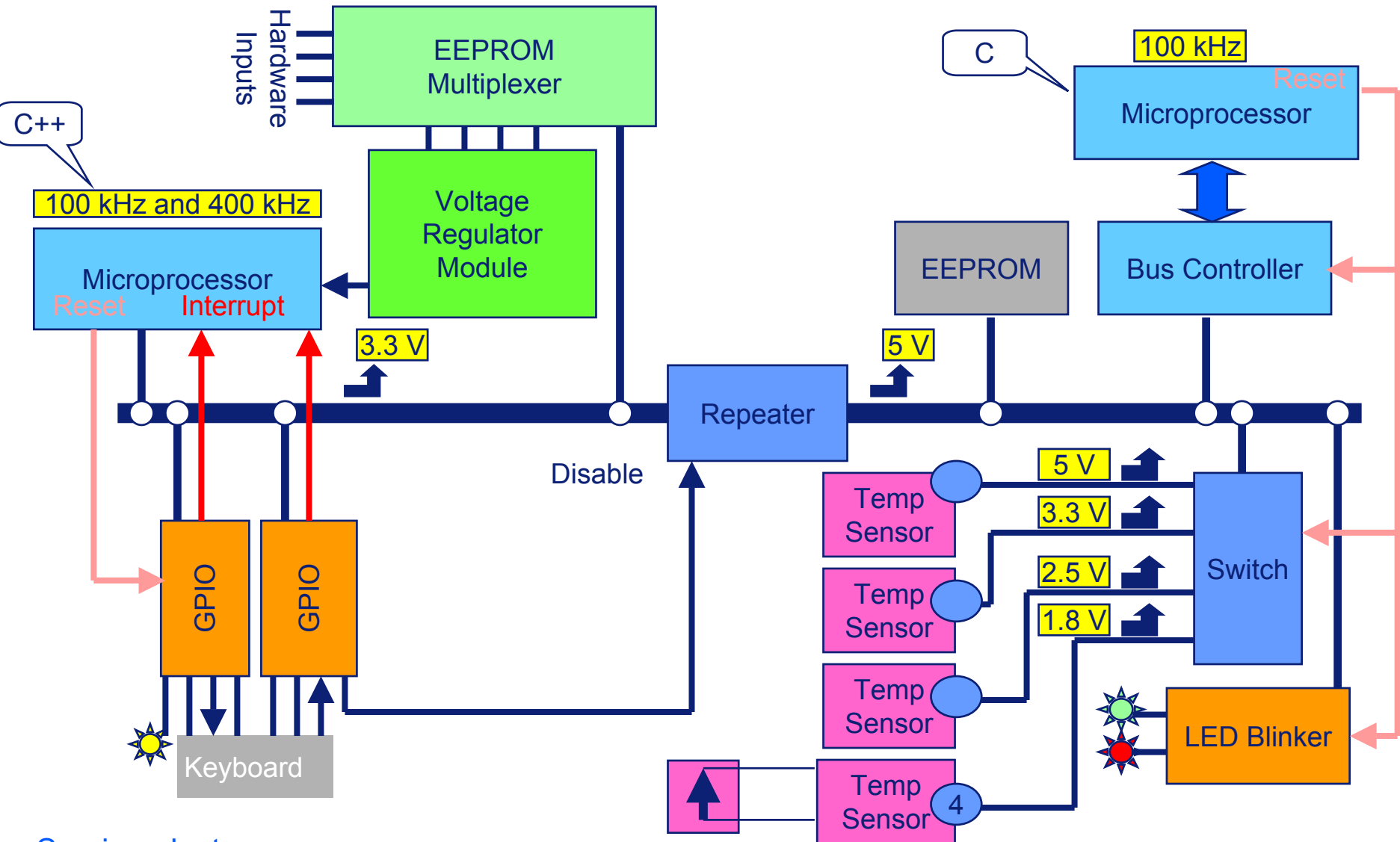


# Typical I<sup>2</sup>C Bus Arrangement





# Complex I<sup>2</sup>C Bus Arrangement



# I<sup>2</sup>C Bus Features

- Only 2 bus lines required: data (SDA) and clock (SCL)
- Each device connected to the bus is software addressable by a unique address
- 2 modes: Master-Transmitter and as Master-Receiver
- Multi-master capable protocol:
  - collision detection
  - arbitration
- Serial bi-directional data transfers:
  - 100 kbit/s                      Standard-mode
  - 400 kbit/s                      Fast-mode
  - 3.4 Mbit/s                      High-speed mode
- Maximum bus capacitance = 400 pF (without repeaters) which is about 20 – 30 devices or 10 ft of wire

# I<sup>2</sup>C Bus Benefits

- Well known bus:
  - Created and developed by Philips
  - More than 20 years of existence
  - Has become a world-wide standard
- Standard adopted by all the industry:
  - Computing
  - Networking
  - Automotive
  - Industrial
  - Telecom
  - Consumer
- Used in many types of applications:
  - PC
  - DVD
  - Cell Phones
  - Printers
  - Set Top Boxes
  - PDA
- Adopted by a lot of leading High-Tech companies
  - Intel
  - IBM
  - Compaq
  - Nokia
  - Cisco
  - HP
- Life of products: designed to stay in the market several years

# I<sup>2</sup>C Designer Benefits

- No need to design bus interfaces because the I<sup>2</sup>C-bus interface is already integrated on-chip.
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined.
- The same IC types can often be used in many different applications.
- ICs can be added to or removed from a system without affecting any other circuits on the bus.
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced.
- Software development time can be reduced by assembling a library of reusable software modules.

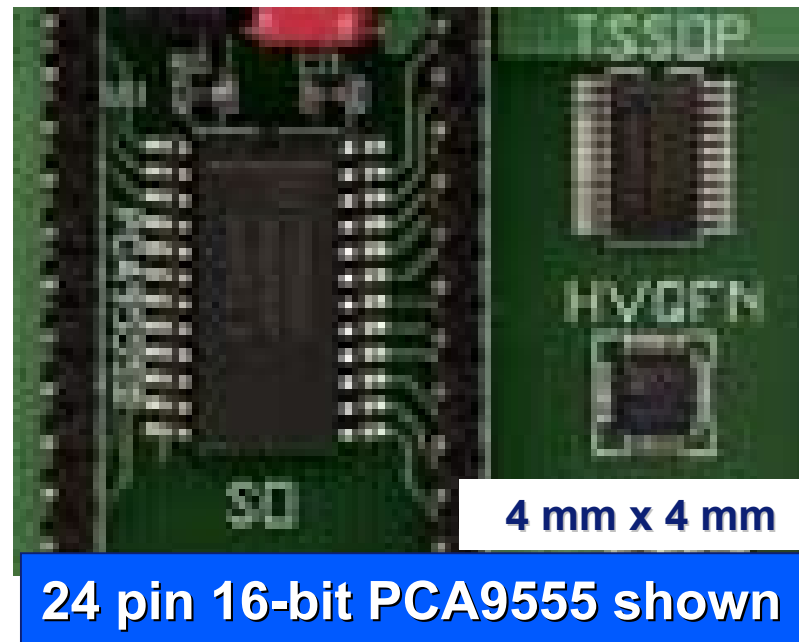
# I<sup>2</sup>C Manufacturer Benefits

- Simplicity: 2 wire protocol
  - Minimum inter connections
  - Minimum footprint
  - Simpler, smaller and less expensive PCB
- Robustness of the protocol
  - Completely integrated protocol
  - No need for address decoding and “glue logic”
  - Interrupt oriented architecture
  - Multi-master capable
- Upgrade path:
  - Speed: 100 kHz → 400 kHz
  - Modular architecture allowing easy design and architecture updates and upgrades

# Technical

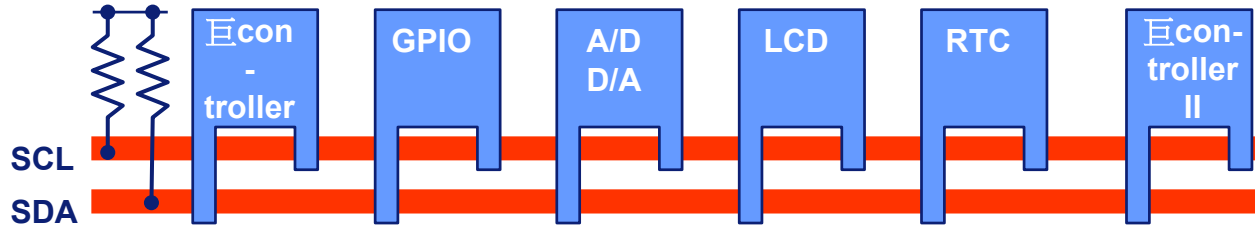
# I<sup>2</sup>C Product Characteristics

- Package Offerings  
Typically DIP, SO, SSOP, TSSOP and/or HVQFN packages
- Frequency Range  
Older devices 100 kHz operation  
Newer devices operating up to 400 kHz
- Operating Supply Voltage Range  
2.3 to 5.5 V or  
3.0 to 3.6 V with 5 V tolerance
- Operating temperature range  
Typically -40 to +85 °C  
Some 0 to +70 °C
- Hardware address pins  
Typically three ( $A_0$ ,  $A_1$ ,  $A_2$ ) are provided to allow up to eight of the identical device on the same I<sup>2</sup>C bus but sometimes due to pin limitations there are fewer address pins



# I<sup>2</sup>C Bus Basics - Address and Data

The master always sends the SCL (clock) signal.

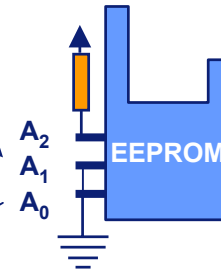


New devices or functions can be easily 'clipped on' to an existing bus!

Each device is addressed individually by software with a unique address that can be modified by hardware pins.

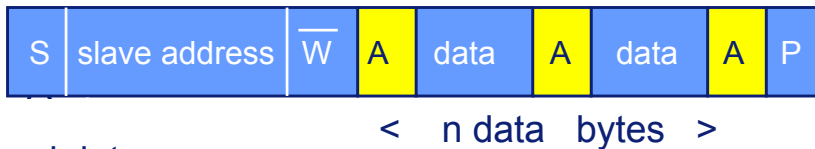
1010A<sub>2</sub>A<sub>1</sub>A<sub>0</sub>R/W

1010100R/W



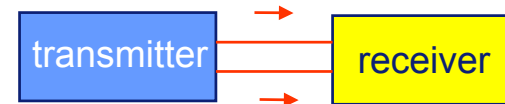
The open drain/collector outputs provide for a "wired-AND" connection that allows devices to be added or removed without impact and always require a pull-up resistor.

Write data

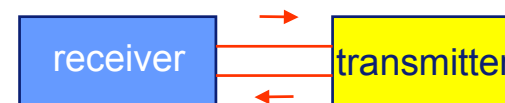
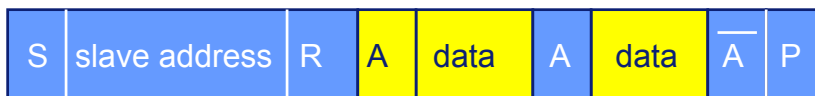


Master

Slave



Read data

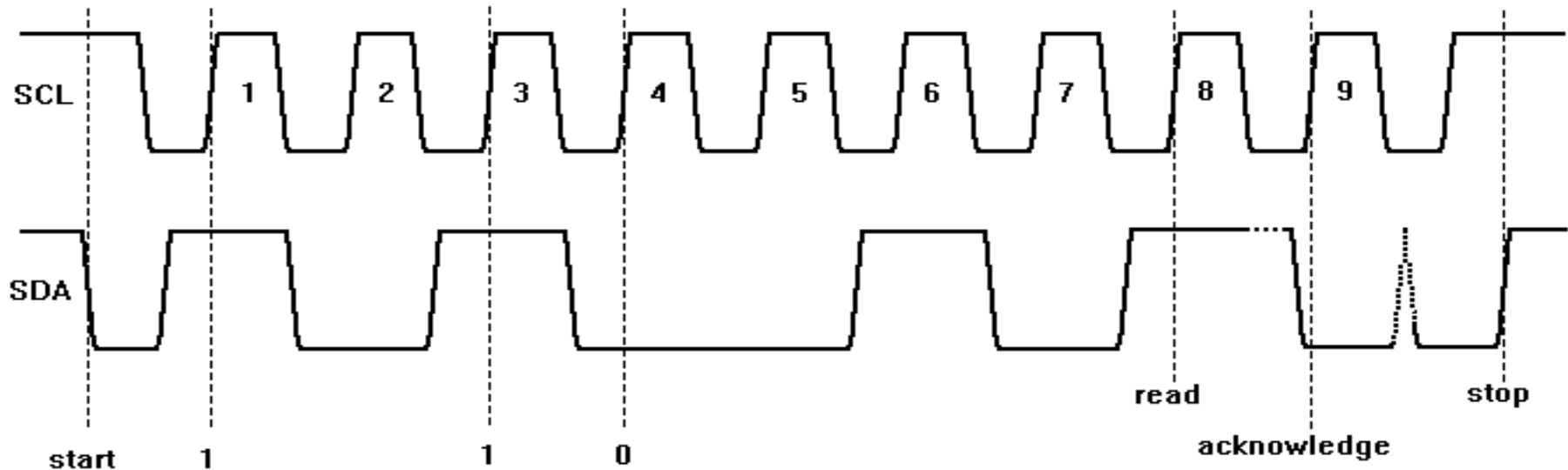


S = Start condition  
A = Acknowledge  
P = Stop condition

R/W = read / write not  
A = Not Acknowledge



# I<sup>2</sup>C Bus Basics - Bus Operation

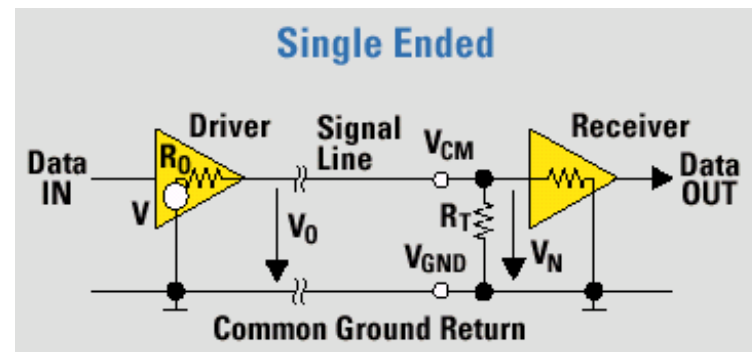
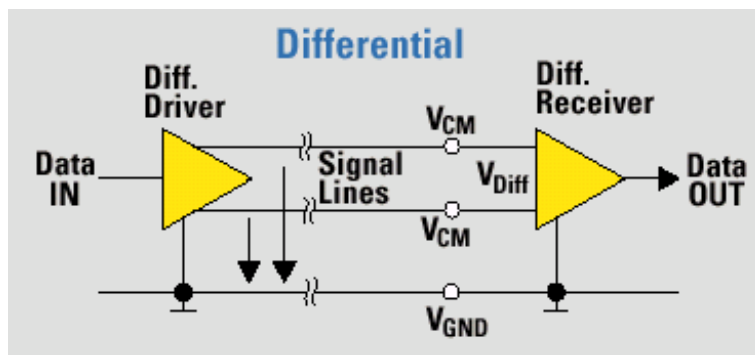


The SCL falling edge 'requests' data when reading, or 'advises' data coming when writing  
 The SDA data changes during the SCL low and is used during or just after the SCL rising edge

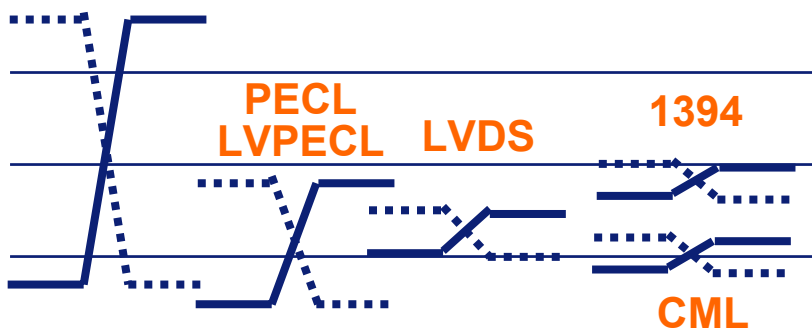
## Typical bus communication waveforms

The I<sup>2</sup>C specification and other useful application information can be found  
 on Philips Semiconductors I<sup>2</sup>C web site at  
[www.semiconductors.philips.com/i2c](http://www.semiconductors.philips.com/i2c)

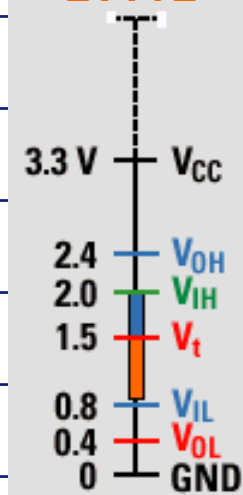
# Typical Signaling Characteristics



RS422/485



LVTTL



LVT  
LVC

I<sup>2</sup>C

I<sup>2</sup>C

SMBus

I<sup>2</sup>C

GTL+

5 V

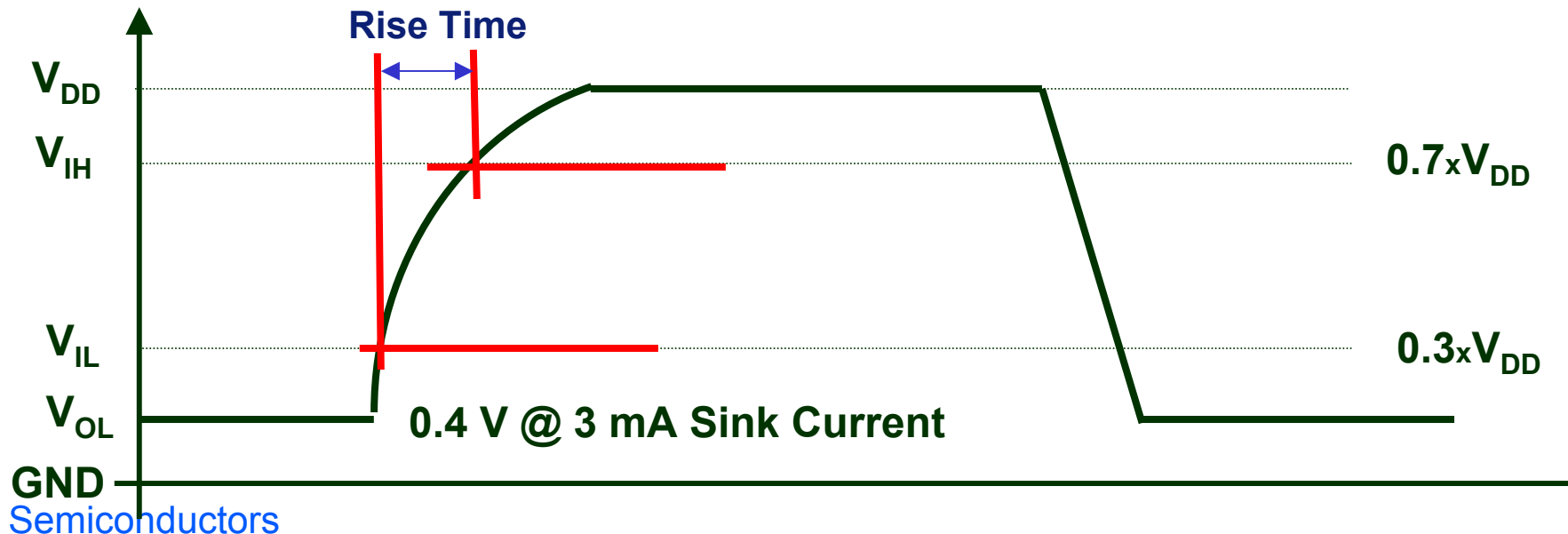
3.3 V

2.5 V

GTL  
GTL<sub>P</sub>

## I<sup>2</sup>C by the numbers

	Standard-Mode	Fast-Mode	High-Speed-Mode	
Bit Rate (kbits/s)	0 to 100	0 to 400	0 to 1700	0 to 3400
Max Cap Load (pF)	400	400	400	100
Rise time (ns)	1000	300	160	80
Spike Filtered (ns)	N/A	50	10	
Address Bits	7 and 10	7 and 10	7 and 10	



# I<sup>2</sup>C Signal Conversion

These microcontrollers have **I<sup>2</sup>C and UART (RS-232)** ports to allow conversion

- P87C6xxx2 family (661 has two byte oriented I<sup>2</sup>C interfaces)
- P87C55x
- P87LPC76x family
- P89C66x
- P89LPC932 and future LPC9xx products

These microcontrollers have **I<sup>2</sup>C and SPI** ports to allow conversion

- XA
- 87C51MX (future product)
- 89LPC9xx (future product)

These microcontrollers and USB devices allow a two device conversion between **I<sup>2</sup>C and USB**

- PDIUSB12 + P89C66x -> 100 kHz I<sup>2</sup>C and USB1.1
- ISP1181 + P89C66x -> 100 kHz I<sup>2</sup>C and USB1.1
- ISP1581 + P89LPC932 -> 400 kHz I<sup>2</sup>C and USB2.0

These ucontrollers have **I<sup>2</sup>C and CAN** ports to allow conversion

- P87C591 - 8 bit solution
- PXA-C37 - 16 bit solution

Products from > [www.semiconductors.philips.com/microcontrollers](http://www.semiconductors.philips.com/microcontrollers)

Support > [www.PhilipsMCU.com/products/standard/microcontrollers/support/feedback/](http://www.PhilipsMCU.com/products/standard/microcontrollers/support/feedback/)  
Semiconductors

# Device Overview

# Philips I<sup>2</sup>C Logic Devices

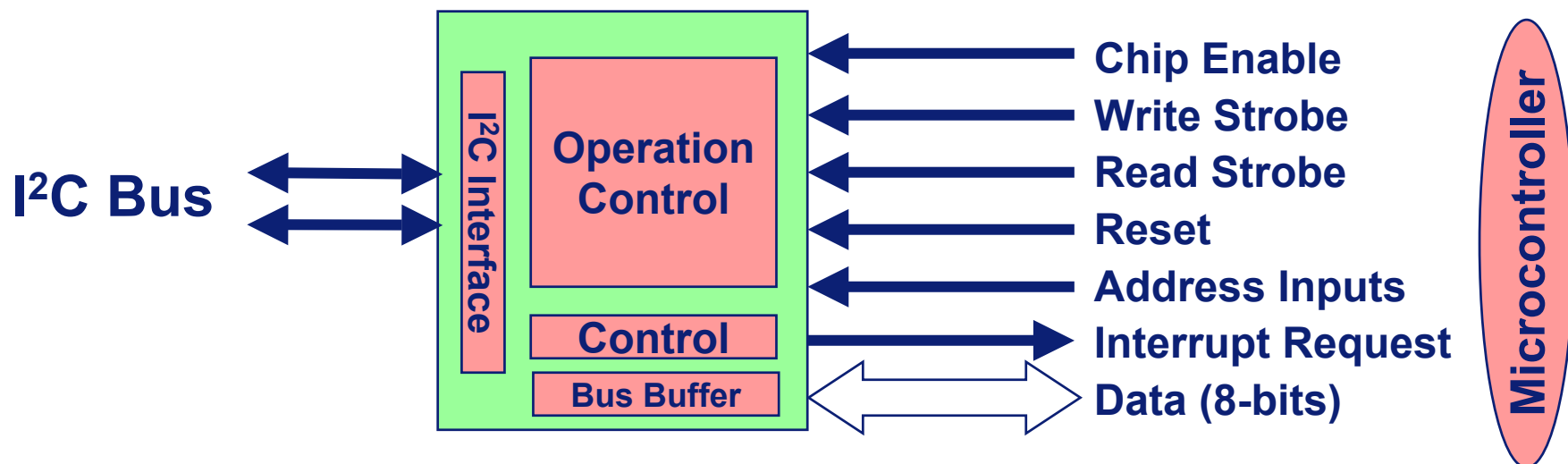
- Bus Controllers
- Temperature Sensors
- I/O Expanders
- LED Blinkers
- Serial EEPROMs
- DIP Switches
- Multiplexers and Switches
- Repeaters/Hubs/Extenders
- Segment Drivers
- Analog/Digital Converters

**I<sup>2</sup>C Logic devices are broken down into 10  
different categories**

**Philips offers over 63 different I<sup>2</sup>C Logic devices**

# Bus Controllers

# Parallel Bus to I<sup>2</sup>C Bus Controller



## FEATURES

- Provides both master and slave functions.
- Controls all the I<sup>2</sup>C bus specific sequences, protocol, arbitration and timing
- Internal oscillator (PCA9564 only)
- Hardware Reset pin and Power On Reset \ (POR)

## KEY POINTS

- Serves as an interface between most standard parallel-bus microcontrollers/ microprocessors and the serial I<sup>2</sup>C bus.
- Allows the parallel bus system to communicate with the I<sup>2</sup>C bus

	Voltage range	Max I <sup>2</sup> C freq	Clock source	Parallel interface
PCF8584	4.5 - 5.5V	90 kHz	External	3 MHz - Slow
PCA9564	2.3 - 3.6V w/5V tolerance	320 kHz	Internal	50 MHz - Fast



# Application – Add I<sup>2</sup>C Bus Port



- The PCA9564 converts 8-bit parallel data into a multiple master capable I<sup>2</sup>C port for microcontrollers, microprocessors, custom ASICs, DSPs, etc., that need to interface with I<sup>2</sup>C or SMBus components.

# Bus Controller vs Bit-banging

## Hardware I<sup>2</sup>C

**Disadvantages:** additional cost

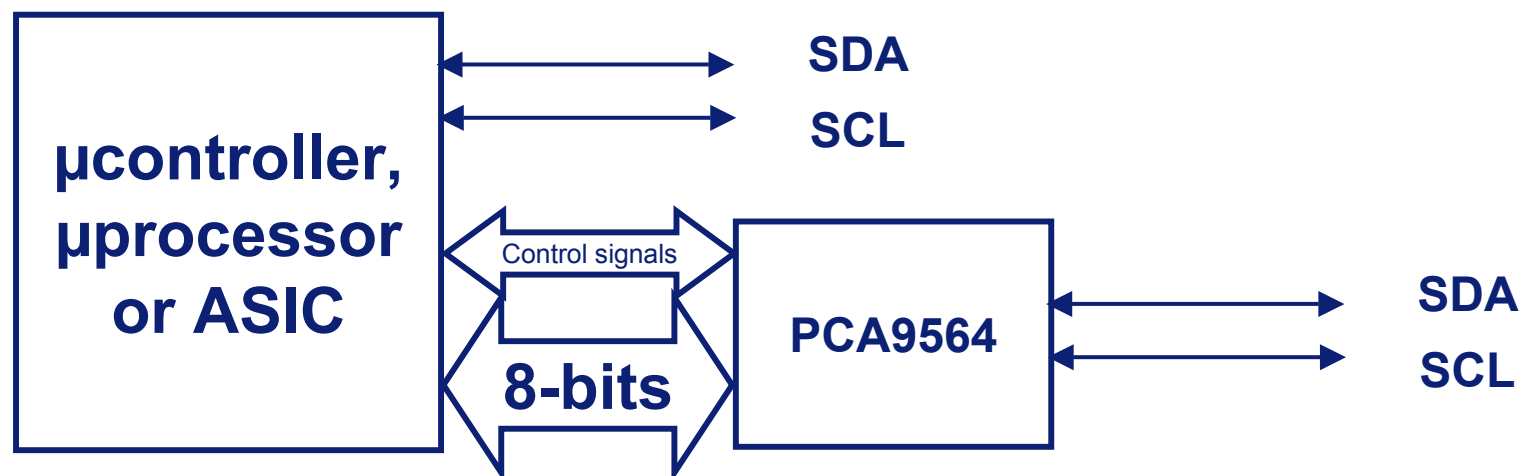
**Advantages:** frees up the micro to perform other tasks, multi-master capability, glitch filters, bus error detection and recovery, can easily be added to most microcontrollers, simple code (code for a hardware I<sup>2</sup>C is relatively simple to write (to write a byte, just load the I2CDAT register with a byte and the hardware does the rest) but you may need to take into consideration all the different error conditions (such as lost arbitration, etc))

## Bit-banging

**Disadvantages:** ties up the micro during the transmission and very difficult to use in a multi-master environment

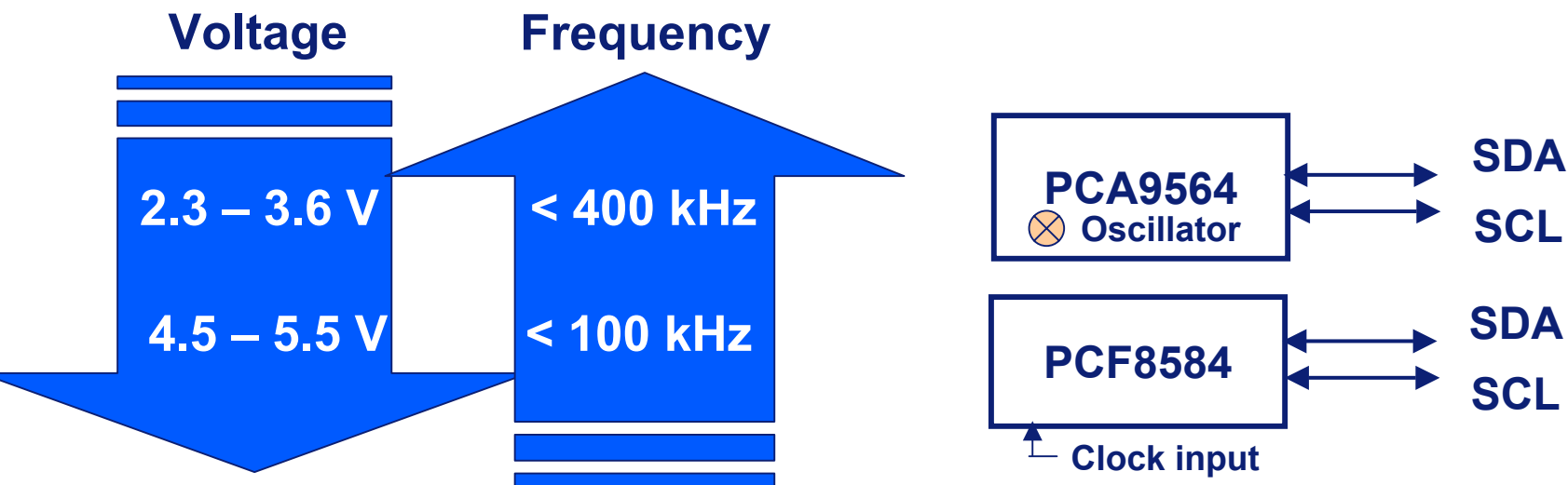
**Advantages:** inexpensive, can be incorporated into any micro and very little code required (code required for bit-banging an 80C51 micro is only about 50 bytes)

# Application – Add additional I<sup>2</sup>C Bus Ports



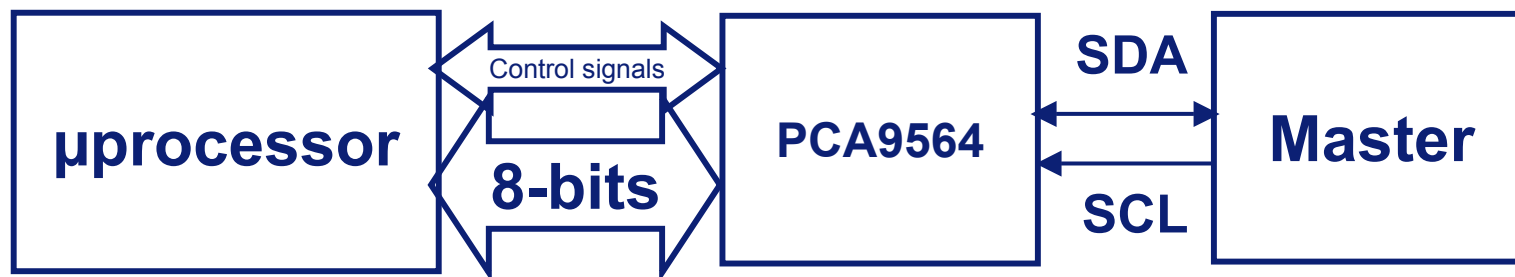
- The PCA9564 can be used to convert 8-bit parallel data into additional multiple master capable I<sup>2</sup>C port for microcontrollers, microprocessors, custom ASICs, DSPs, etc., that already have an I<sup>2</sup>C port but need one or more additional I<sup>2</sup>C ports to interface with more I<sup>2</sup>C or SMBus components or components that cannot be located on the same bus (e.g., 100 kHz and 400 kHz slaves).

# Application – Lower Voltage & Higher Frequency Migration Path for PCF8584



- The PCA9564 does the same type of parallel to serial conversion as the PCF8584. Although not footprint compatible, the PCA9564 provides improvements such as:
  - Operating at 3.3 V and 2.5 V voltage nodes
  - Allows interface with I<sup>2</sup>C or SMBus components at speeds up to 400 kHz.
  - The built-in oscillator provides a cost effective solution since the external clock input is no longer required.
  - Parallel data can be exchanged at speeds up to 50 MHz allowing the use of faster processors. The PCA9564 is optimized for the Intel 8051 architecture.

# Application – Convert 8 bits of parallel data into I<sup>2</sup>C serial data stream



- Functioning as a slave transmitter, the PCA9564 can convert 8-bit parallel data into a two wire I<sup>2</sup>C data stream. This prevents having to run 8 traces across the entire width of the PC board.

# Temperature Sensors

# I<sup>2</sup>C Temperature Sensors - Industrial

**The human hand is capable  
of sensing temperature  
changes within 2°C**



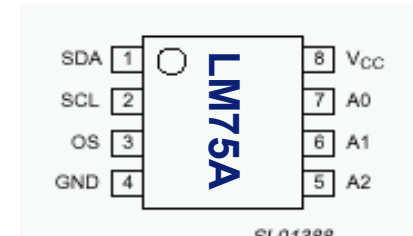
Our temperature sensors have a resolution up to 0.125°C

## FEATURES

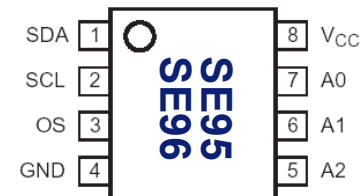
- Temperature range of – 55 to 125 °C
- Open drain interrupt output

## KEY POINTS

- Sense temperature via I<sup>2</sup>C
- SE95 accurate to ± 1 °C from 0 to 100 °C
- SE96 accurate to ± 0.5 °C from 0 to 100 °C

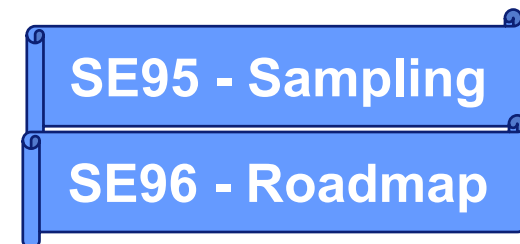


## Digital Temperature Sensor and Thermal Watchdog™

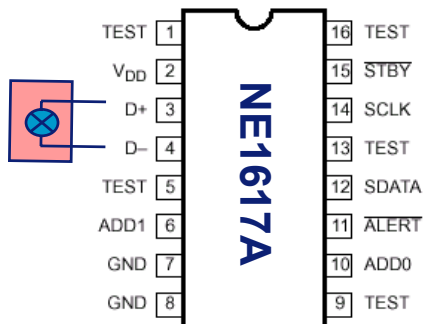


## Ultra High Accuracy Digital Temperature

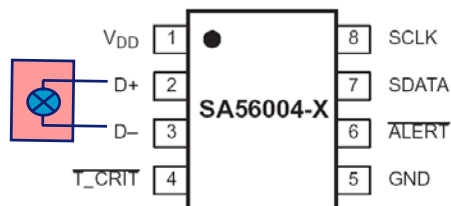
## Sensor and Thermal Watchdog™



# I<sup>2</sup>C Temperature Sensors - PC



**I<sup>2</sup>C Temperature Monitor**

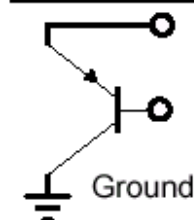


**±1°C Accurate, Remote/Local  
Digital Temperature Sensor with  
Over Temperature Alarms**

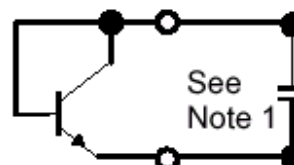
## FEATURES

- High temperature accuracy
- SA56004 has eight address

**Remote Sensor:**



**μP On-Board PNP Transistor**

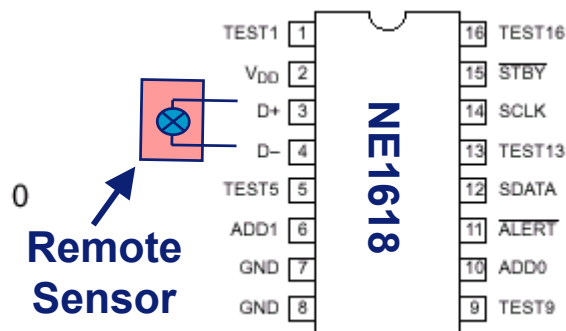


**or Discrete NPN Transistor**

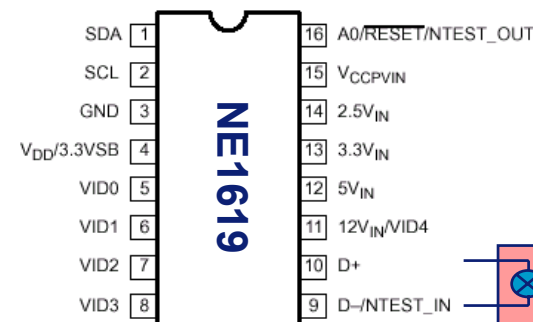
**New!**

## KEY POINTS

- Sense temperature and/or monitor voltage via I<sup>2</sup>C
- Remote sensor can be internal to microprocessor



**High Accuracy Temp Monitor**



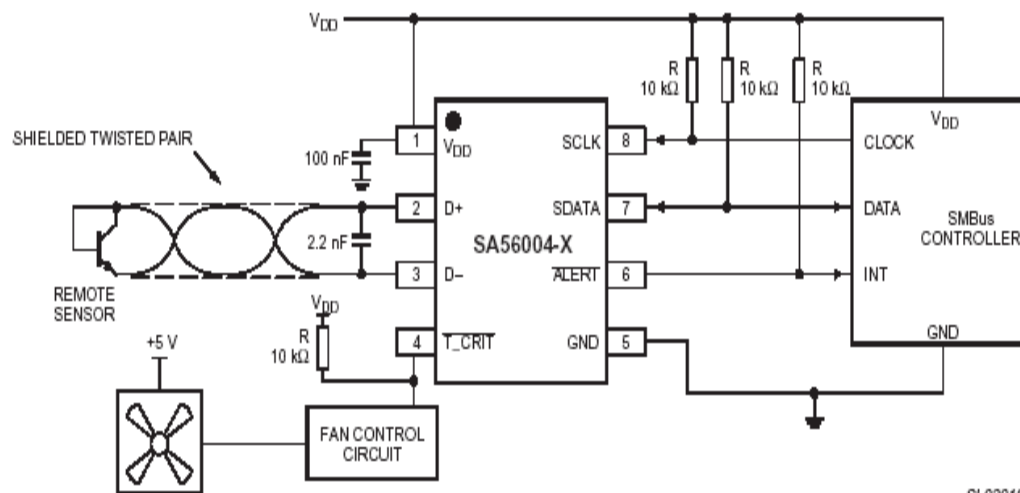
**I<sup>2</sup>C Temperature and Voltage  
Monitor (Heceta4)**



# SA56004 Application

## APPLICATIONS

- System thermal management in laptops, desktops, servers and workstations
- Computers and office electronic equipment
- Electronic test equipment & instrumentation
- HVAC
- Industrial controllers and embedded systems



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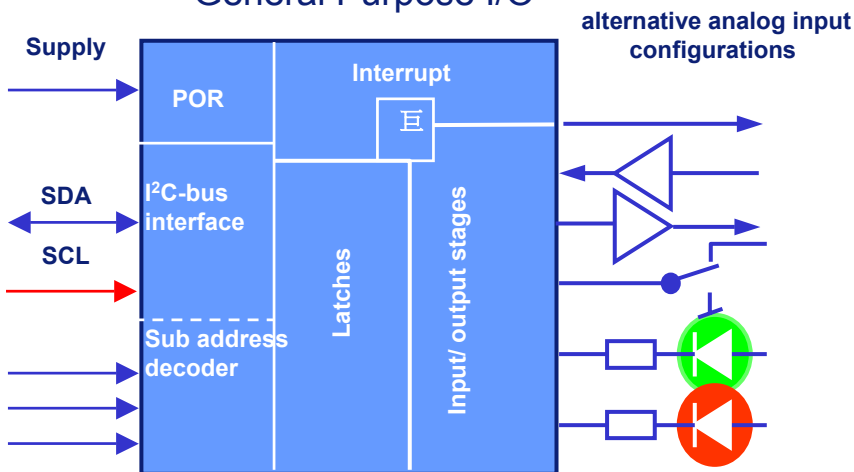
## FEATURES

- On-chip local and remote microprocessor thermal diodes or diode connected transistors temperature sensing within  $\pm 1$  °C
- Offset registers available for adjusting the remote temperature accuracy
- Programmable under/over temperature alarms: ALERT and T\_CRIT
- SMBus 2.0 compatible interface, supports TIMEOUT and 100/400 kHz I<sup>2</sup>C interface
- 11-bit, 0.125 °C resolution
- 8 different device addresses are available for server applications. The SA56004-ED/EDH with marking code ARW is address compatible with the National LM86, the MAX6657/8 and the ADM1032.

# I/O Expanders

# Quasi Output I<sup>2</sup>C I/O Expanders

General Purpose I/O



## KEY POINTS

- Transfers keyboard, ACPI Power switch, keypad, switch or other inputs to microcontroller via I<sup>2</sup>C bus
- Expand microcontroller via I<sup>2</sup>C bus where I/O can be located near the source or on various cards
- Use outputs to drive LEDs, sensors, fans, enable and other input pins, relays and timers
- Quasi outputs can be used as Input or Output without the use of a configuration register
- The PCA9501 has 6 address pins, allowing up to 64 devices to share the same I<sup>2</sup>C Bus.
- Application Note, AN469 GPIO Selection, discusses pros and cons of GPIOs

# of Outputs	Interrupt	2Kbit EEPROM	Interrupt and 2Kbit EEPROM
<b>Quasi Output (20-25 ma sink and 100 uA source)</b>			
8	PCF8574/74A	PCA9500/58	PCA9501
16	PCF8575/75C	-	-

# Quasi Output I<sup>2</sup>C I/O Expanders - Registers

- To program the outputs



Multiple writes are possible during the same communication

- To read input values

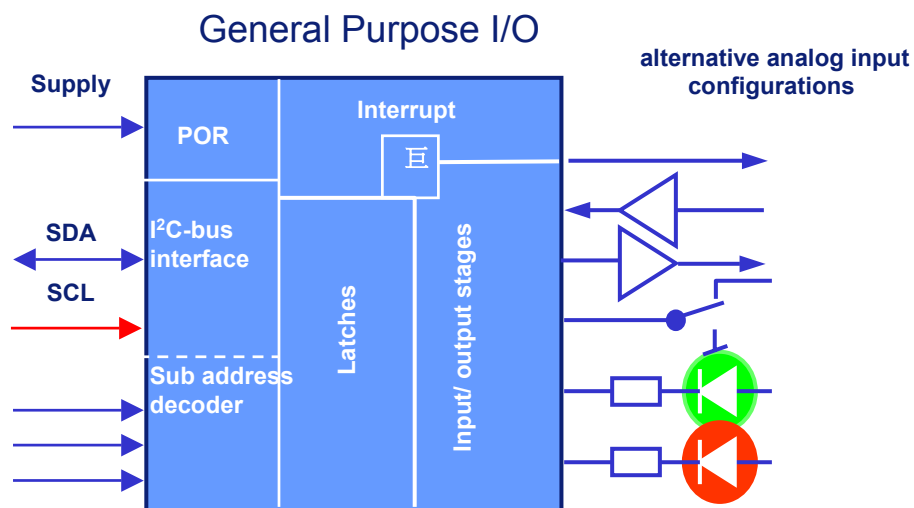


Multiple reads are possible during the same communication

- Important to know

- At power-up, all the I/O's are HIGH (except PCF8575C); Only a current source to  $V_{DD}$  is active
- Upper transistor is on for one clock cycle to provide strong pull-up and allow for faster rising edge rate
- I/O's should be HIGH before using them as inputs

# Totem Pole Output I<sup>2</sup>C I/O Expanders



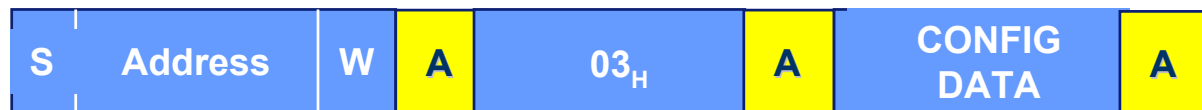
## KEY POINTS

- Transfers keyboard, ACPI Power switch, keypad, switch or other inputs to microcontroller via I<sup>2</sup>C bus
- Use totem pole outputs to drive LEDs, sensors, fans, enable and other input pins, relays and timers
- Extra command byte needed for Input, Output, Polarity and I/O Configuration
- Application Note, AN469 GPIO Selection, discusses pros and cons of GPIOs

# of Outputs	None	Reset	Interrupt	Interrupt and Reset
Totem Output (20-25 ma sink and 10 mA source)				
4	PCA9536			PCA9537
8		PCA9557	PCA9534/54/54A	PCA9538
16	-	-	PCA9535/55	PCA9539

# Totem Output I<sup>2</sup>C I/O Expanders - Registers

- To configure the device



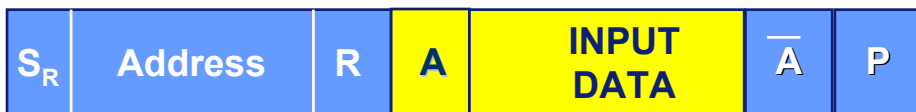
No need to access Configuration and Polarity registers once programmed

- To program the outputs



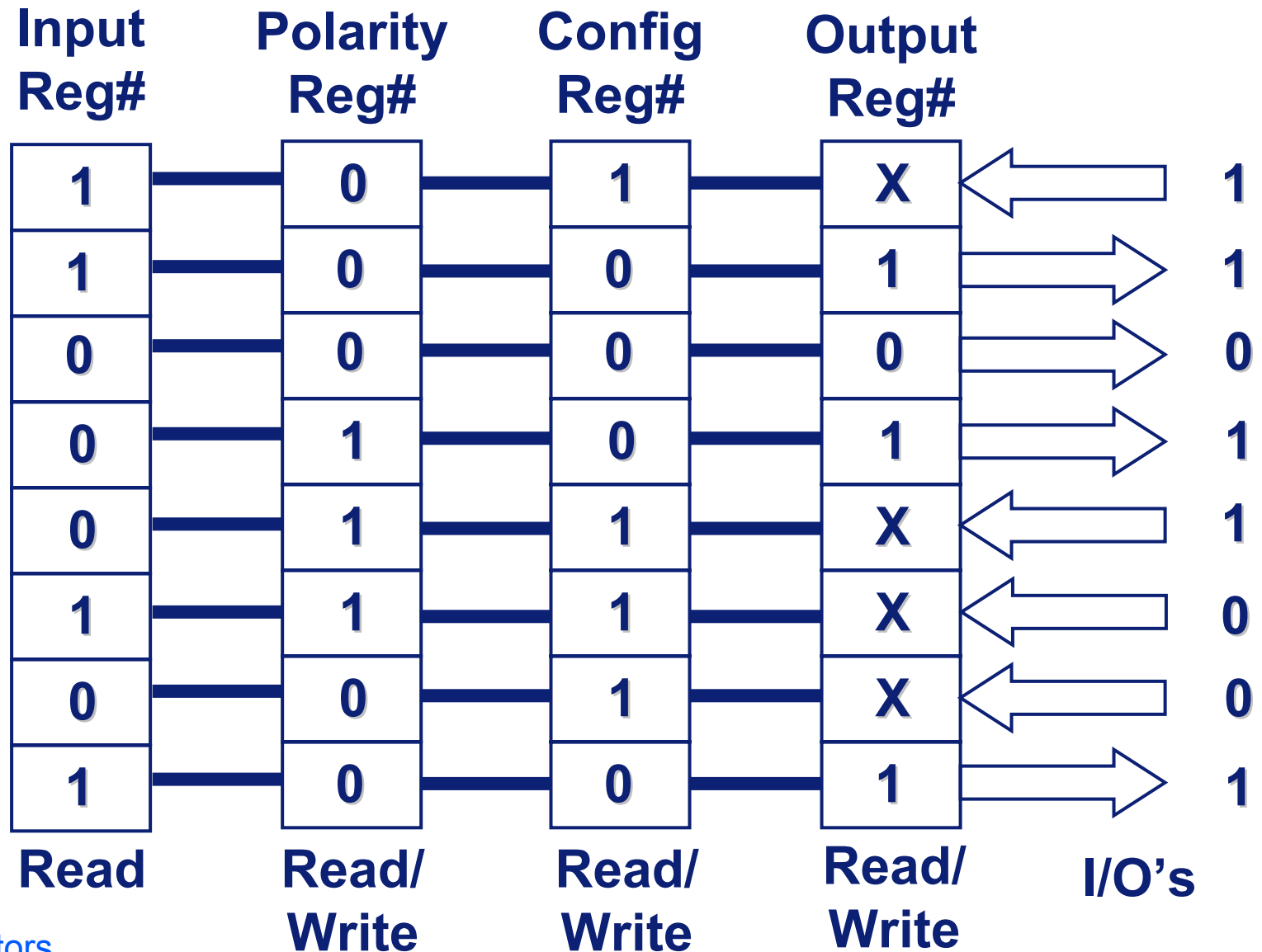
Multiple writes are possible during the same communication

- To read input values



Multiple reads are possible during the same communication

# Totem Pole Output I<sup>2</sup>C I/O Expanders - Example



## 4-bit GPIO

I00	1	8	VCC
I01	2	7	SDA
I02	3	6	SCL
GND	4	5	I03

- Similar to the PCA9554 but only 4 bits in an 8 pin SO or TSSOP package
- Fixed I<sup>2</sup>C address of 1000001R/W

- **PCA9536 4-Bit I<sup>2</sup>C GPIO**

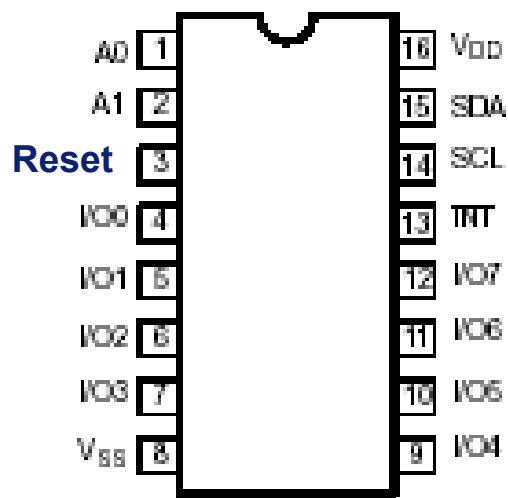


# 4-bit GPIO with Interrupt and Reset

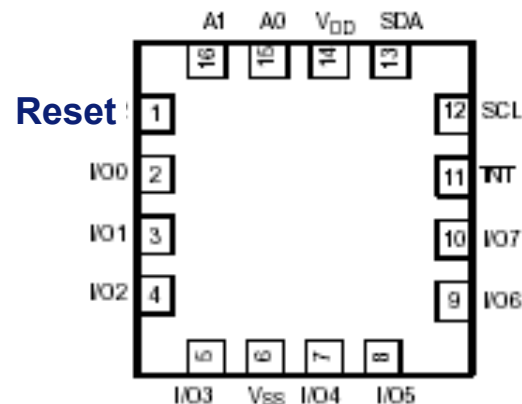
$\overline{\text{RESET}}$	1	10	VCC
I00	2	9	SDA
I01	3	8	SCL
I02	4	7	ANT
GND	5	6	I04

- Similar to the PCA9538 but only 4 bits of GPIO in an 10 pin TSSOP package
- Fixed I<sup>2</sup>C address of 1001001R/W
- **PCA9537 4-Bit I<sup>2</sup>C GPIO with Interrupt and Reset**

# 8-bit GPIO with Interrupt and Reset



SO or TSSOP

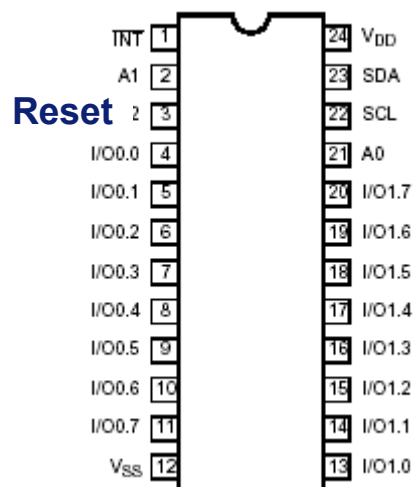


HVQFN

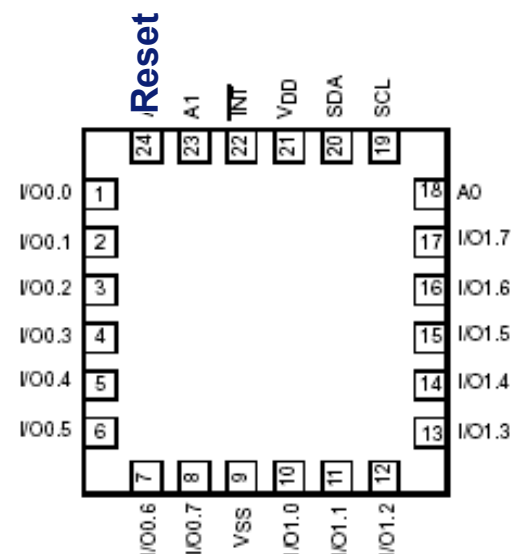
- Based on PCA9534 die with a metal mask option to tie A2 high internally and bring out the POR circuit to the hardware reset pin.
- Polling for input changes is not required since Interrupt output signals master.
- Reset pin is needed for higher bus reliability to allow all devices to be reset should the bus hang up.

## • PCA9538 8-Bit GPIO with Interrupt and Reset

# 16-bit GPIO with Interrupt and Reset



SO and TSSOP



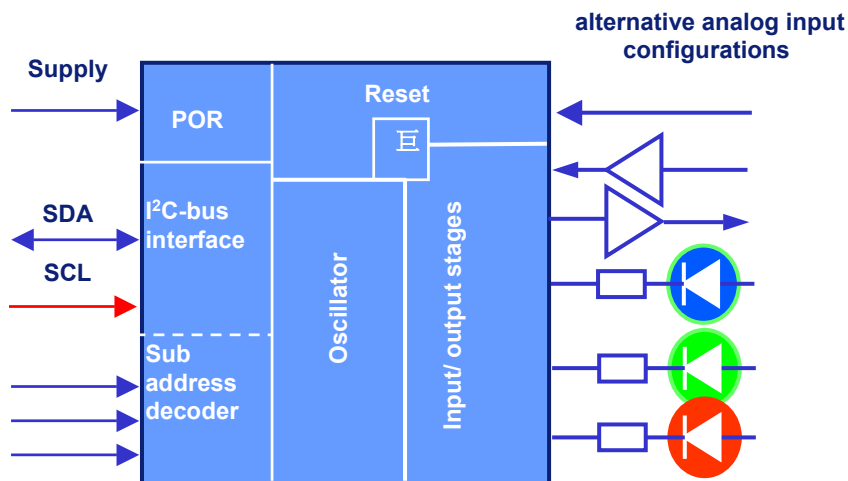
HVQFN

- Based on PCA9535 die with metal mask option to tie A2 high internally and bring out the POR circuit to the hardware reset pin.
- Polling for input changes is not required since Interrupt output signals master.
- Reset pin is needed for higher bus reliability to allow all devices to be reset should the bus hang up.

## • PCA9539 16-Bit GPIO with Interrupt and Reset

# LED Blinkers

# I<sup>2</sup>C LED Dimmers/Blinkers



## KEY POINTS

- I<sup>2</sup>C/SMBus is not tied up by sending repeated transmissions to turn LEDs on and then off to “blink” LEDs.
- Frees up the micro’s timer
- Continues to blink LEDs even when no longer connected to bus master
- Can be used to cycle relays and timers
- Higher frequency rate allows LEDs to be dimmed by varying the duty cycle for Red/Green/Blue color mixing applications.

## FEATURES

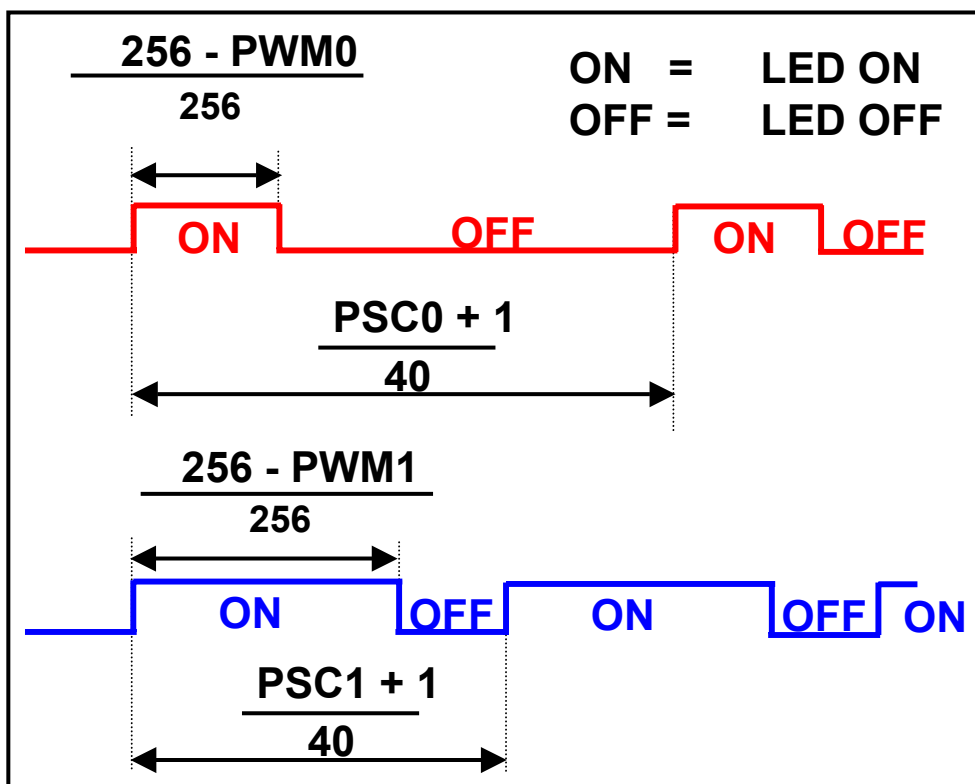
- 25 mA open drain outputs
- Internal oscillator (+/- 15%)
- Two user definable blink rates and duty cycles adjustable between 160 Hz and 1.6 seconds (3x Dimmers) or 40 Hz and 6.4 seconds (5x Blinkers) in 256 steps
- Unused pins can be used for normal GPIO
- Hardware Reset pin and Power On Reset (POR)

# of Outputs	Reset and POR
2	PCA9530/50
4	PCA9533/53
8	PCA9531/51
16	PCA9532/52

Application Note AN264

# PCA955x I<sup>2</sup>C LED Blinkers

	0 (00 <sub>H</sub> )	255 (FF <sub>H</sub> )
Frequency	40 Hz	6.4 s
Duty Cycle	100 %	0.4 %



Input Register(s)

PWM0 (ON Time)

PSC0 (Frequency)

PWM1 (ON Time)

PSC1 (Frequency)

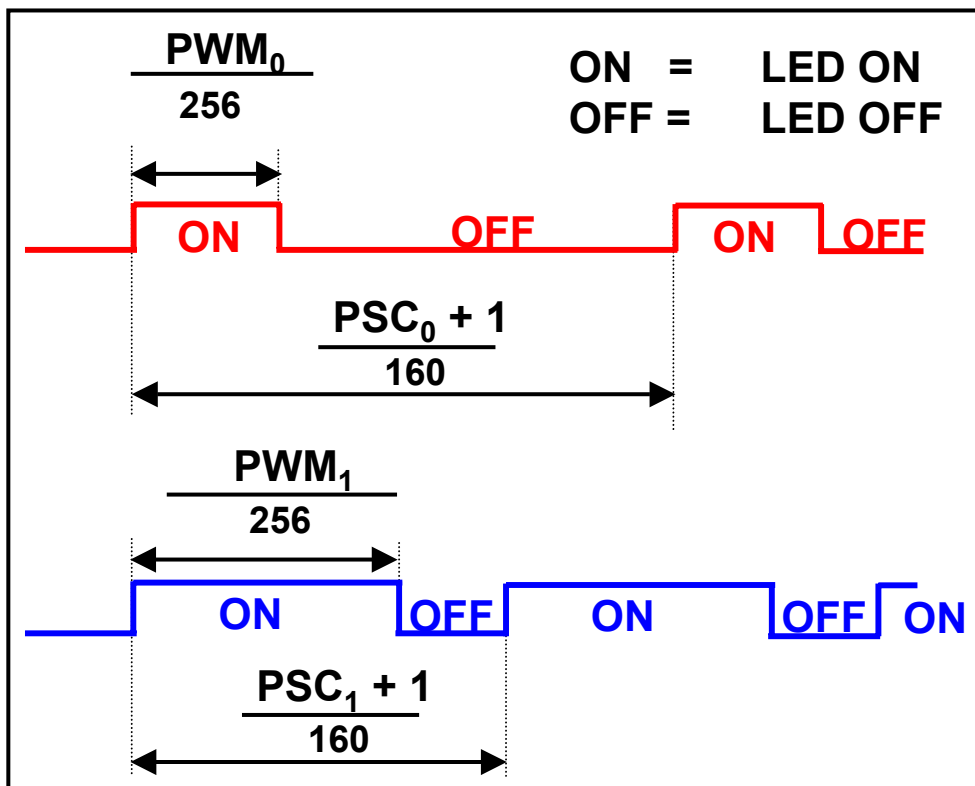
LED Selector

ON, OFF, BR1, BR2

# PCA953x I<sup>2</sup>C LED Dimmers

	0 (00 <sub>H</sub> )	255 (FF <sub>H</sub> )
Frequency	160 Hz	1.6 s
Duty Cycle	0 %	99.6 %

State machine defaults to highest frequency at power on and duty cycle goes from 0% (off) to 99.6% (almost always on) for better dimming control.



ON, OFF, BR1, BR2

# LED Dimmers/Blinkers vs Micros

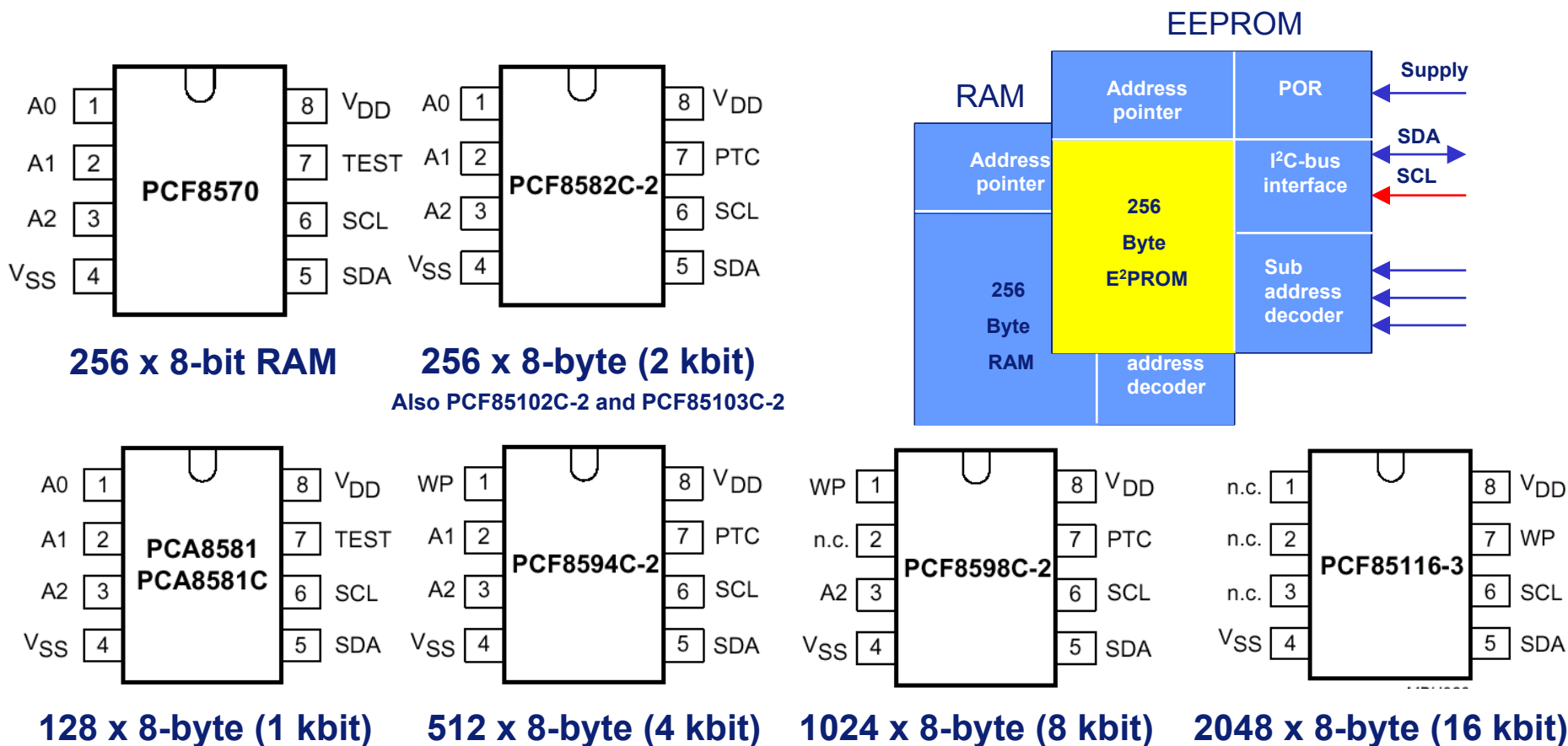
Difference between using a LED Blinker/Dimmer or a micro:

- Easier software generation to control LEDs
  - Don't have to use micro timer
  - Don't have to continually send on and off command to blink or dim LEDs
- Frequency fixed by device, not dependant on processor clock frequency
- I<sup>2</sup>C devices have higher sink current capability per bit and larger sink current capability per device



# Serial EEPROMS

# I<sup>2</sup>C Serial CMOS RAM/EEPROMs



## FEATURES

- Wide voltage range of 2.5 to 5.5V
- 1,000,000 read and write cycles
- 10 year data retention

## KEY POINTS

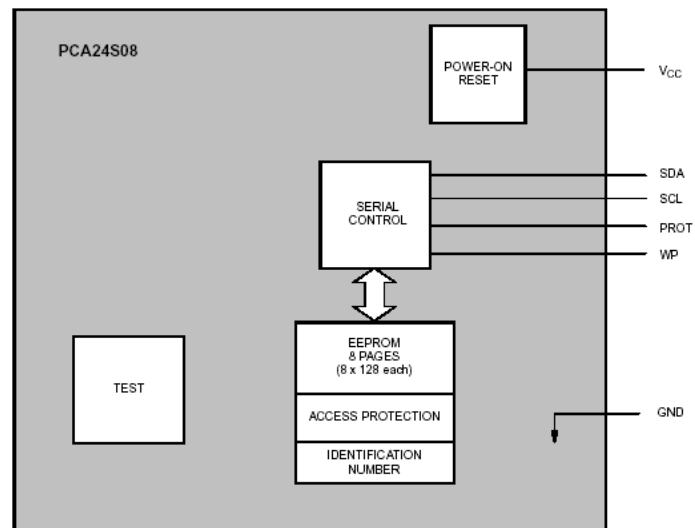
- I<sup>2</sup>C bus is used to read and write information to and from the memory
- Wide voltage range minimizes the number of EEPROMs that need to be in inventory

# 1024 X 8 CMOS Security EEPROM

SYMBOL	NAME AND FUNCTION
NC	No connect
PROT	Protection input
GND	Ground
SDA	Serial data open drain I/O
SCL	Serial clock input
WP	Write protect input
V <sub>CC</sub>	Supply voltage

## FEATURES

- Nonvolatile memory - serial interface
- Compatible with a Standard 24C08 Serial EEPROM
- Programmable access protection to limit reads or writes
- Lock/unlock function
- Highly-reliable EEPROM memory
- 8 k bits (1 k bytes), organized as 8 blocks of 128 bytes
- 16-byte page write, 10 ms write time
- 10 years retention, 100 k write cycle endurance
- Operating temperature range - 40 to +85 °C
- Operating power supply voltage range of 2.5 V to 3.6 V
- Packages offered: SO8 and TSSOP8



## DESCRIPTION

The PCA24S08 functions as a dual access EEPROM with a wired serial port used to access the memory. Access permissions are set from the serial interface side to isolate blocks of memory from improper access.

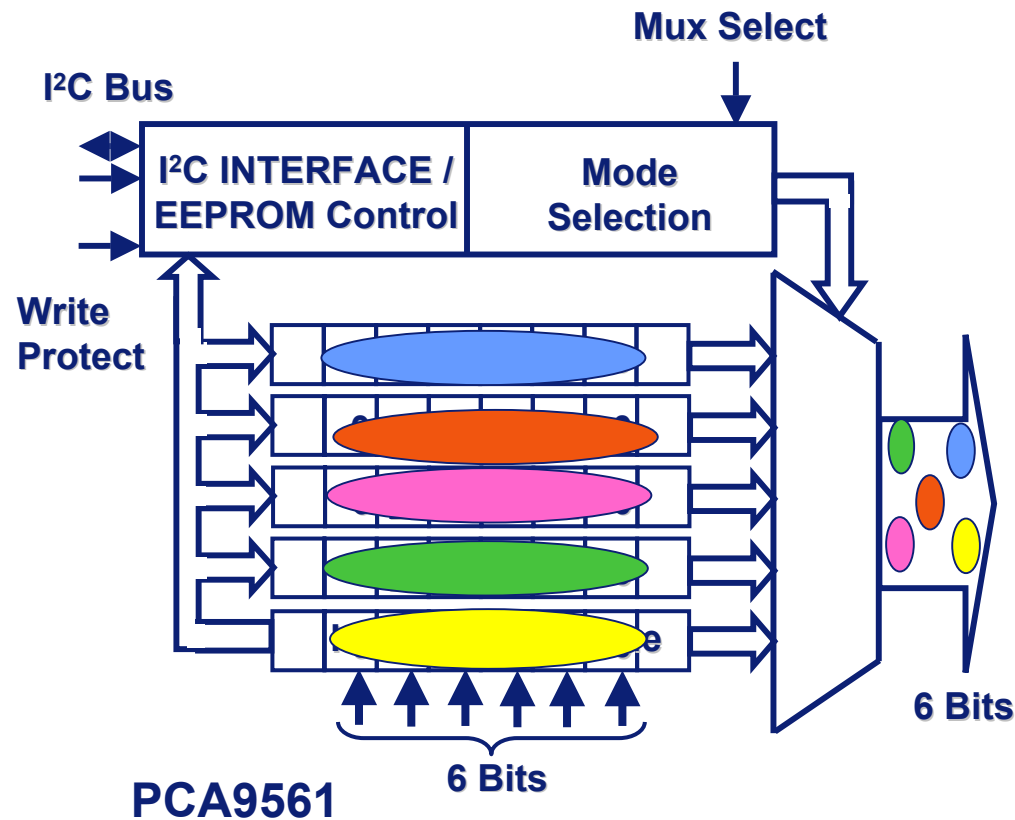
**10101B<sub>2</sub>B<sub>1</sub>**

Only 1 device allowed per bus

**PCA24S08 - 1024 X 8 CMOS EEPROM with access protection**

# DIP Switches

# I<sup>2</sup>C DIP Switches



	# of Pins	# of Non Volatile Registers	# of Register Bits	# of Hardware Input Pins	# of Muxed Outputs	Non-Muxed Output
PCA8550	16	1	5	4	4	YES
PCA9558	28	1	6	5	5	YES
PCA9559	20	1	6	5	5	YES
PCA9560	20	2	6	5	5	YES
PCA9561	20	4	6	6	6	NO

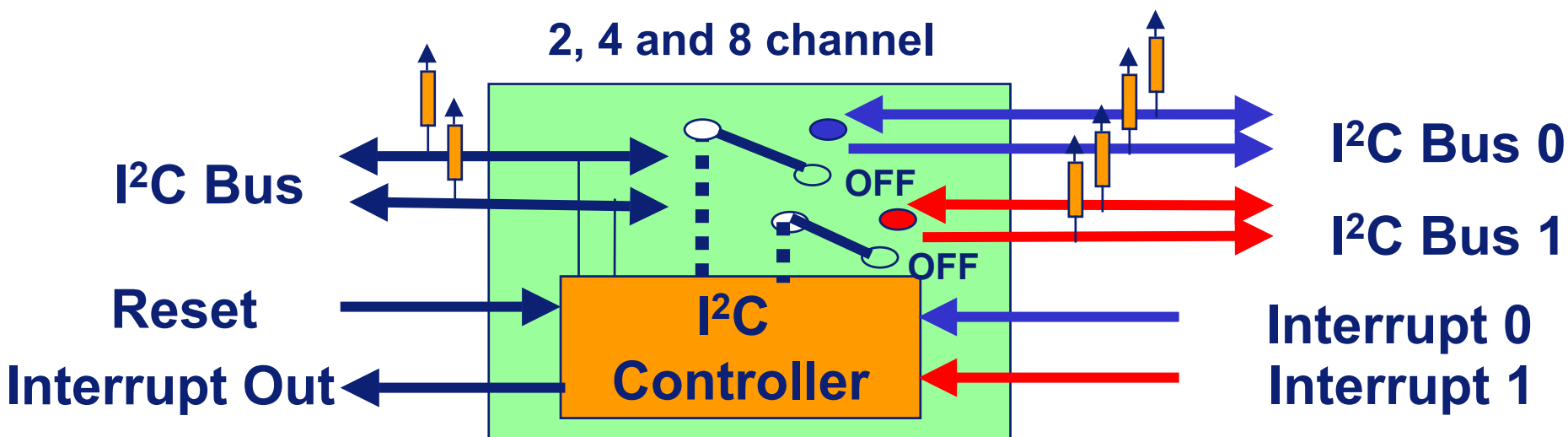
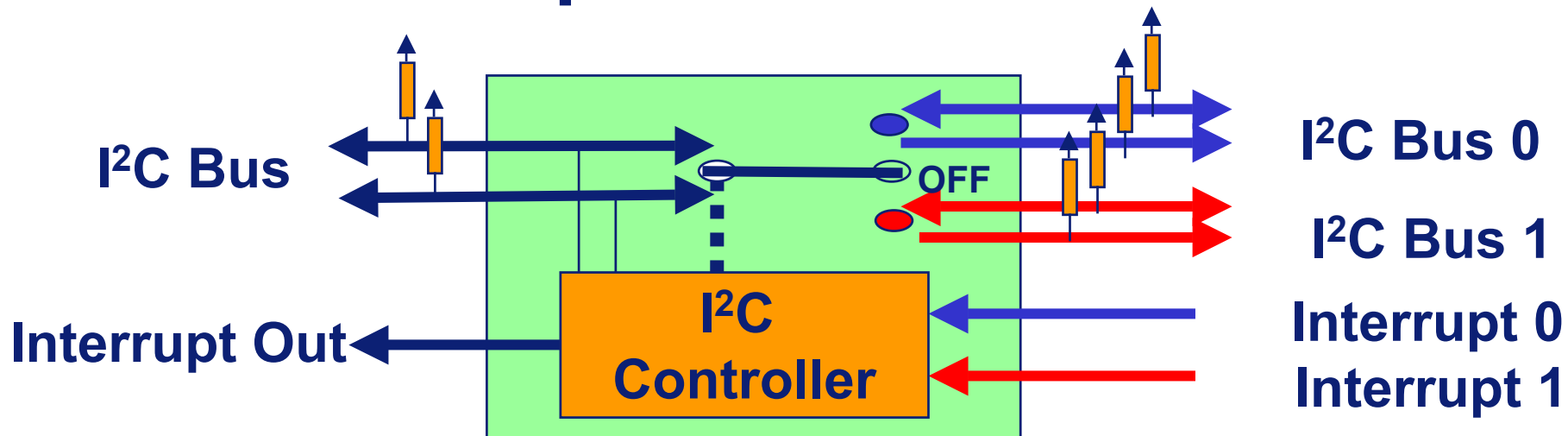
Application Note  
AN250

6 bit output value is dependant on the mux select pin position or command from I<sup>2</sup>C master

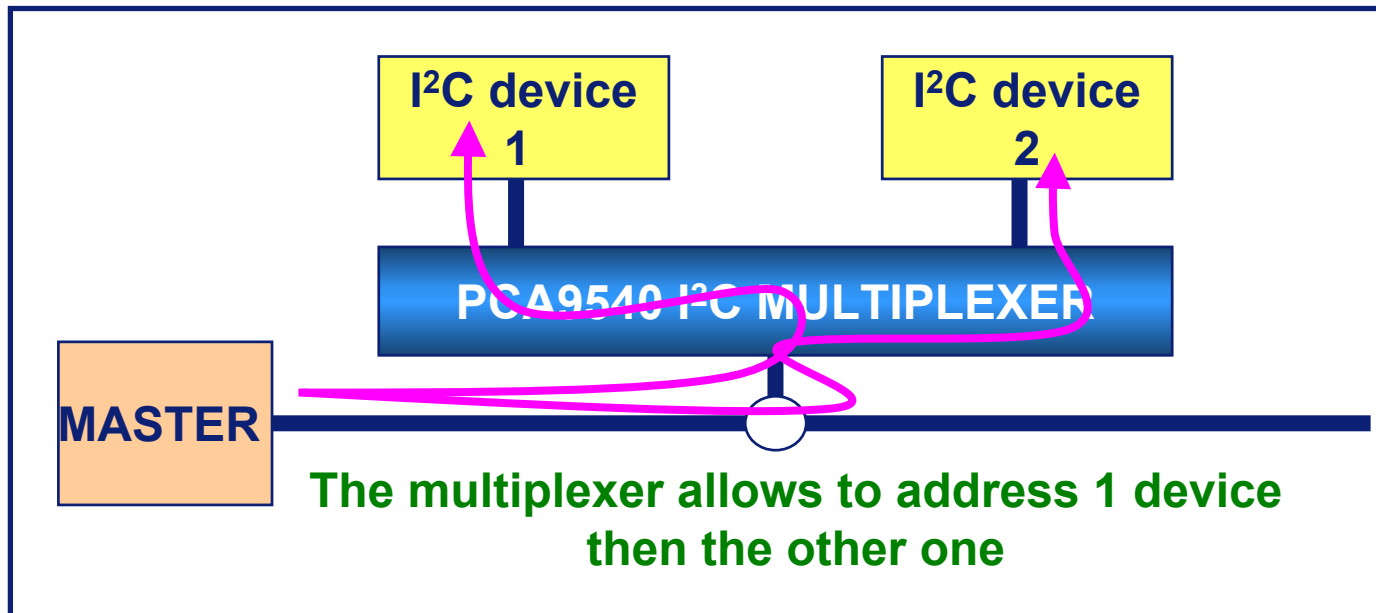
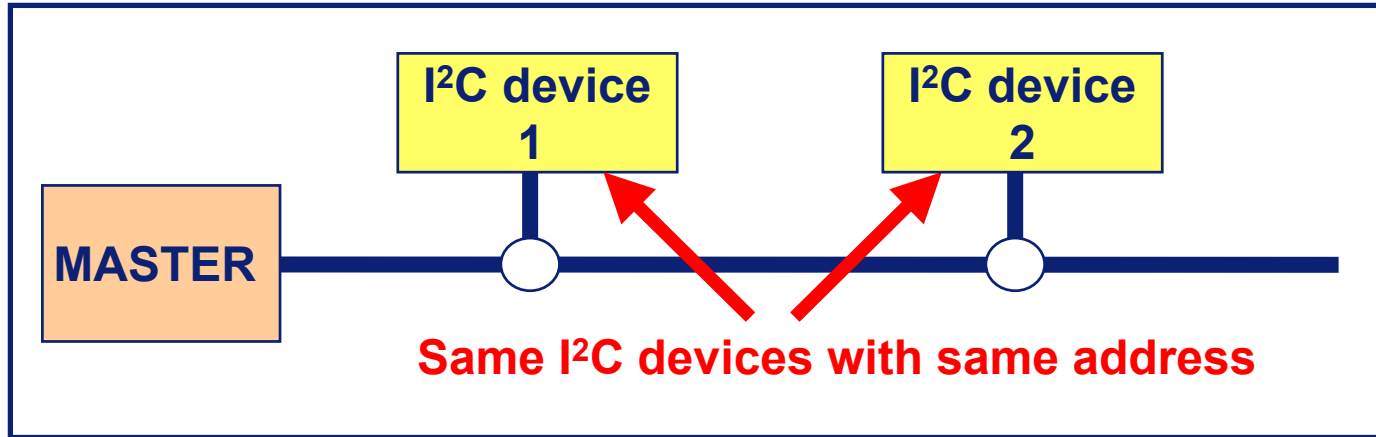
EEPROM 0 is default output

# Multiplexers & Switches

# I<sup>2</sup>C Multiplexers and Switches

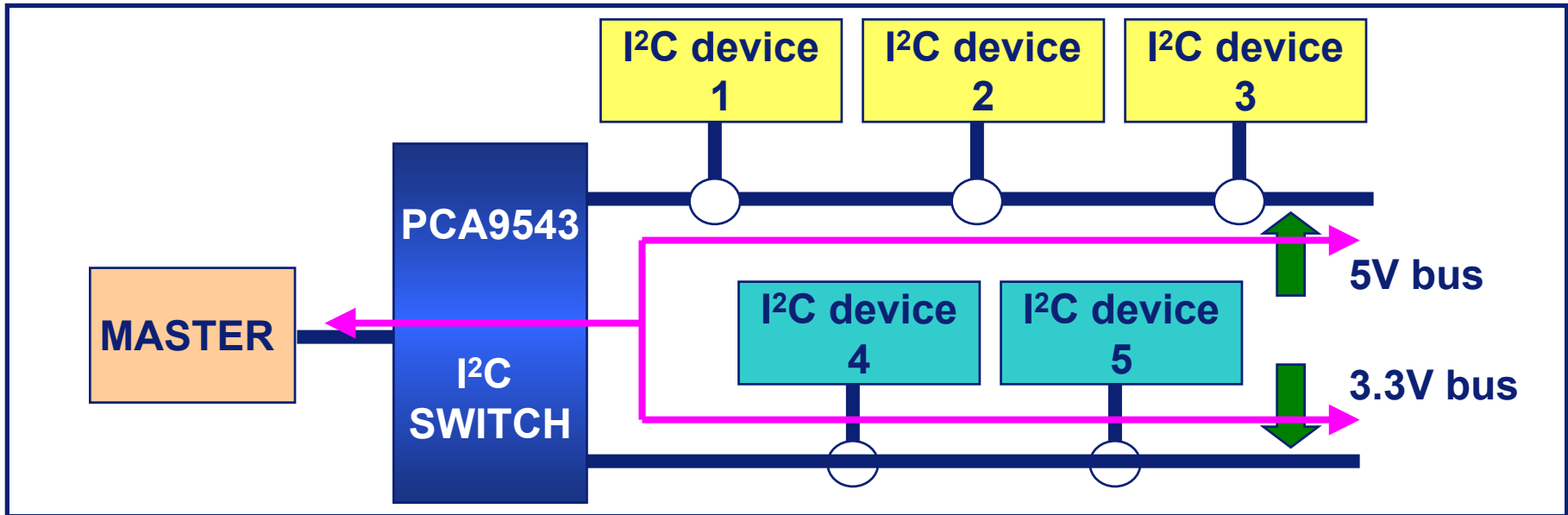
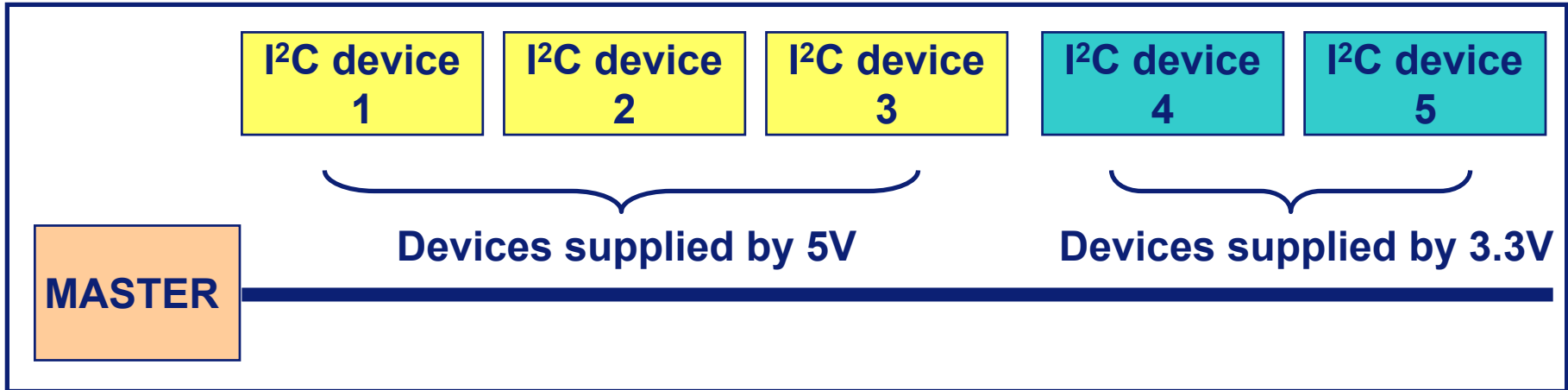


# I<sup>2</sup>C Multiplexers: Address Deconflict

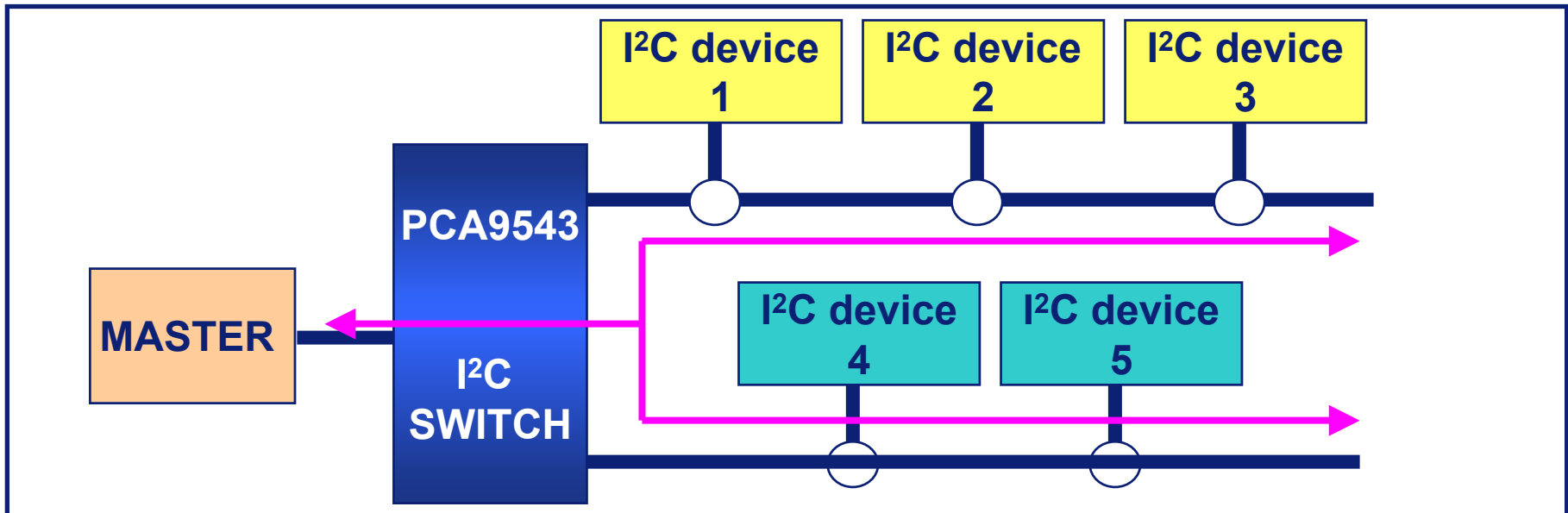
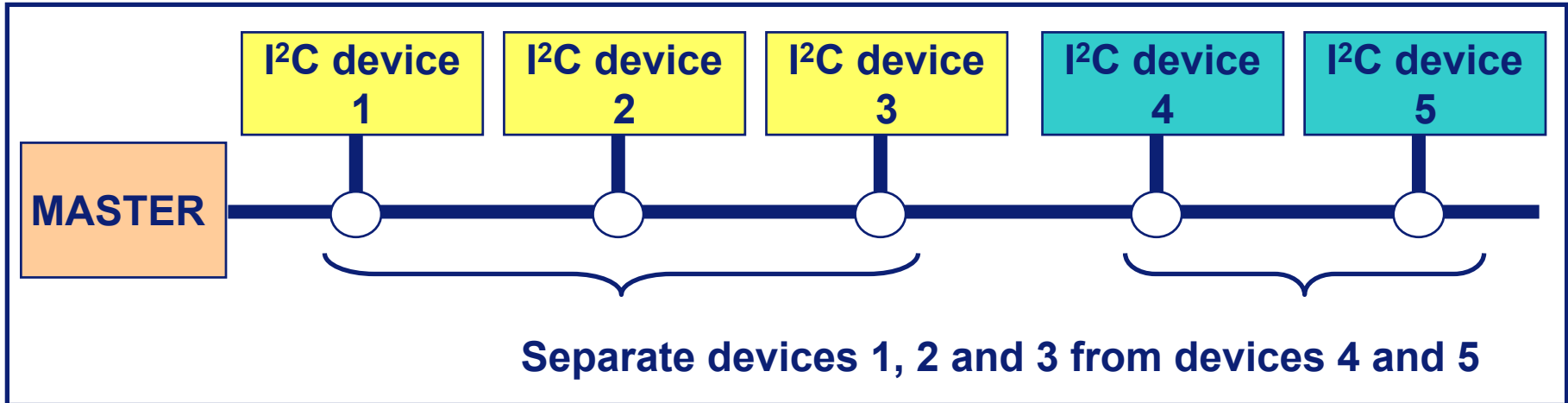




# I<sup>2</sup>C Switches: Voltage Level Shifting

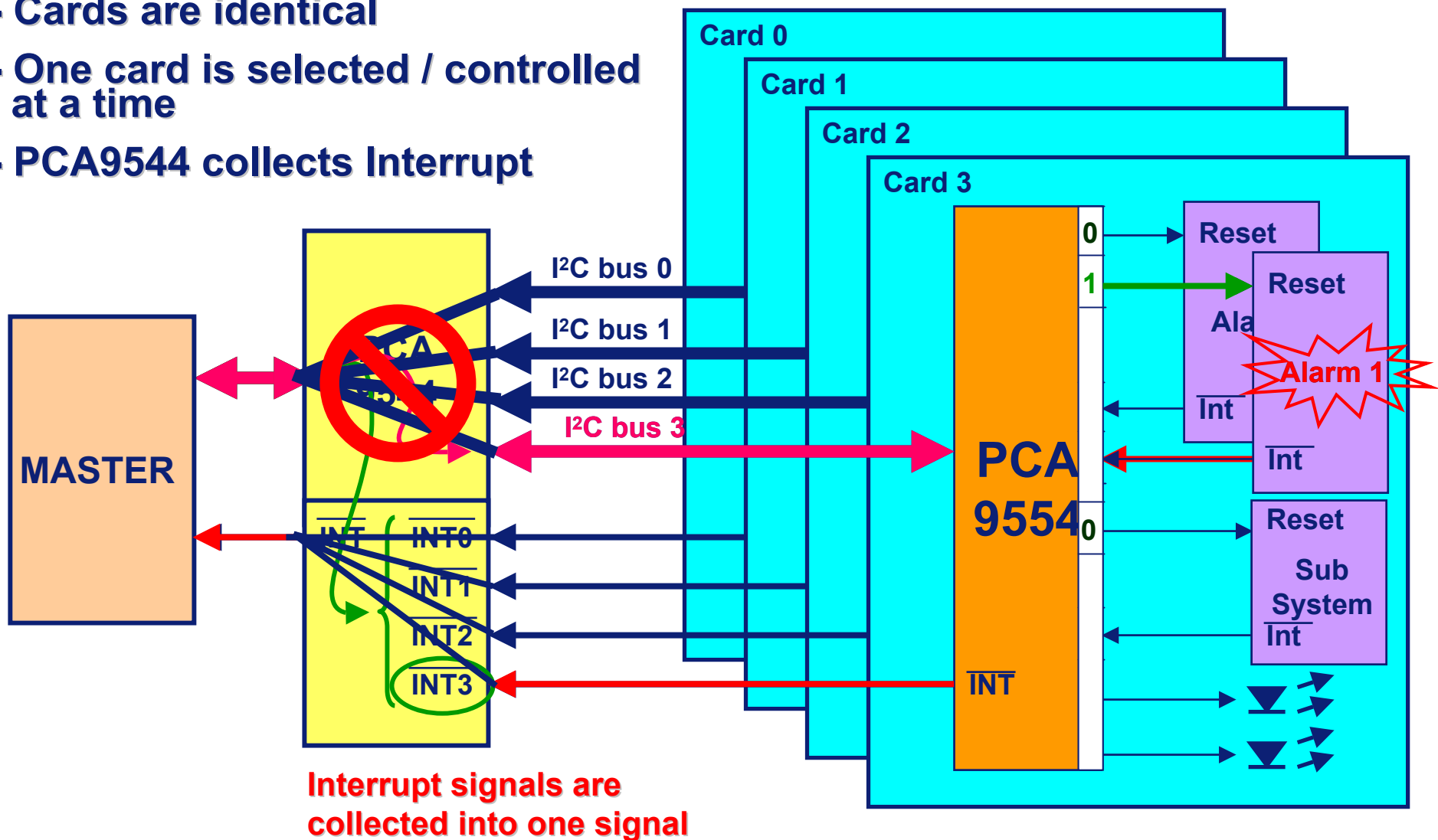


# I<sup>2</sup>C Switches: Branch isolation

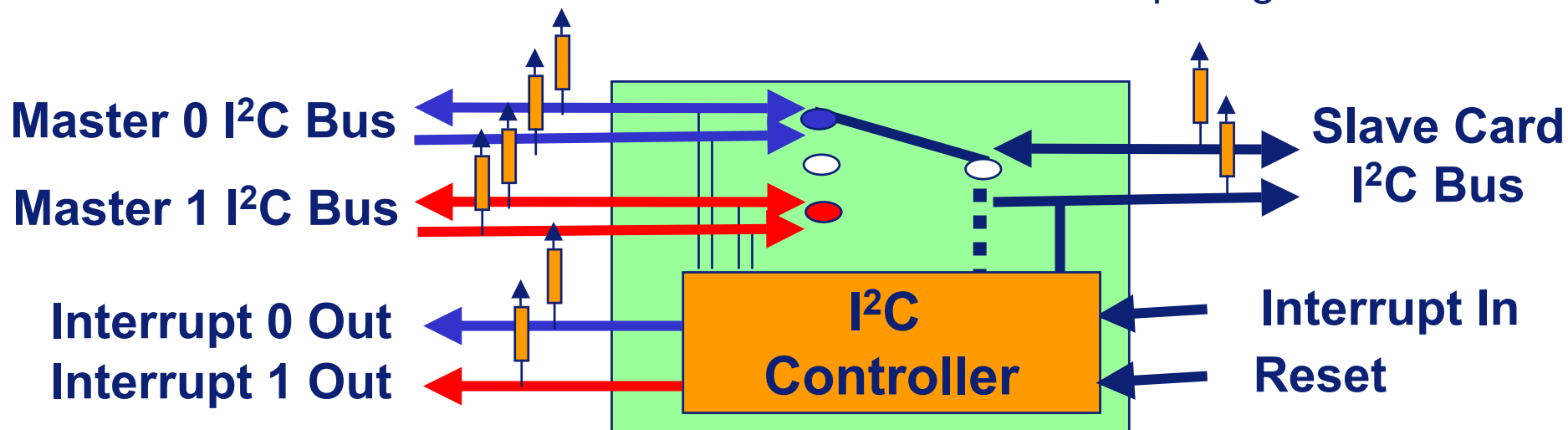


# I<sup>2</sup>C Multiplexers: Multi-card Application

- Cards are identical
- One card is selected / controlled at a time
- PCA9544 collects Interrupt



# 2 to 1 I<sup>2</sup>C Master Selector w/Interrupt Logic and Reset



## FEATURES

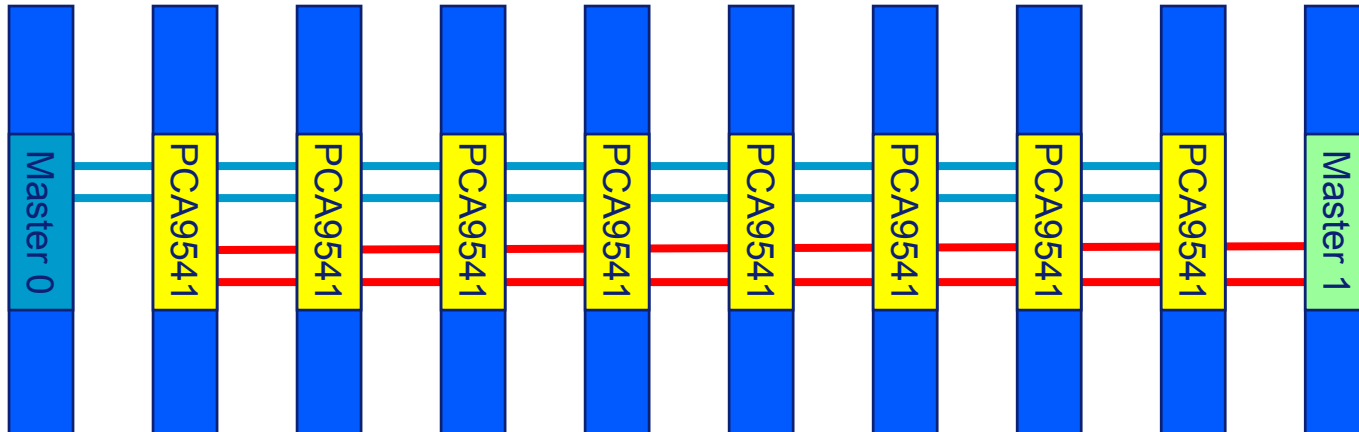
- Select one of two I<sup>2</sup>C masters to a single channel
- I<sup>2</sup>C/SMBus commands used to select channel
- Reset or Power On Reset (POR) resets state machine
- Interrupt outputs also report demultiplexer status
- Sends 9 clock pulses and stop condition to clear slave card prior to transferring master

## KEY POINTS

- Allows primary and backup master to communicate to one downstream slave card.
- Arbitration circuit between bus masters
- Doesn't isolate bus capacitance
- Allows voltage translation between 1.8 V, 2.5 V, 3.3 V and 5 V
- Idle detect for live insertion protection

- **PCA9541/01** - defaults to channel 0 on start-up/reset
- **PCA9541/02** - defaults to channel 0 on start-up/reset after stop condition
- **PCA9541/03** – defaults to off on start-up/reset, master commands channel

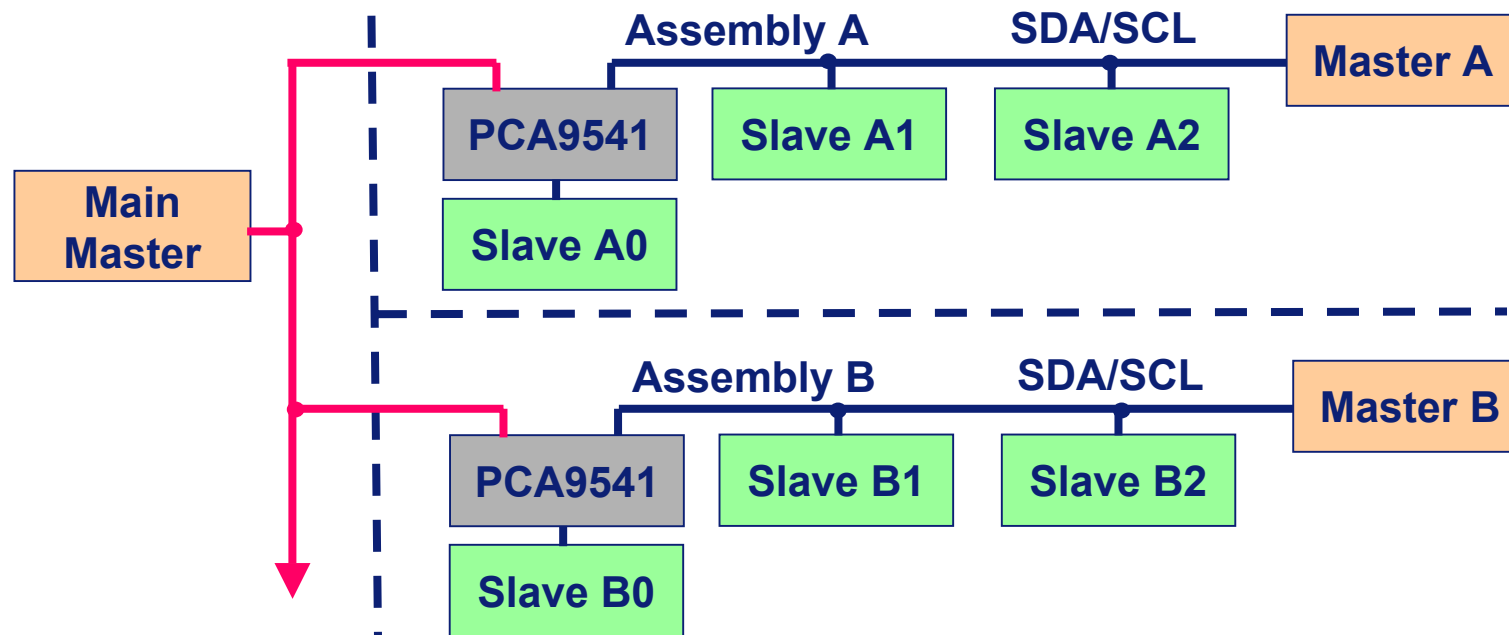
# PCA9541 - Multi-Point Application



In a typical multi-point application, as shown in the diagram, the two masters (e.g., primary and back-up) are located on separate I<sup>2</sup>C buses that connect to multiple downstream I<sup>2</sup>C bus slave cards via a PCA9541 to provide high reliability of the I<sup>2</sup>C bus.

This way one of the controller cards can fail or be removed from the system and control of the line cards is maintained. A bent pin or other hard failure is confined to one bus and control is maintained on the other bus. I<sup>2</sup>C commands are sent via the primary or back-up master and either master at any time can gain control of the slave devices if the other master is disabled or removed from the system. The failed master is isolated from the system and will not affect communication between the on-line master and the slave devices located on the line cards.

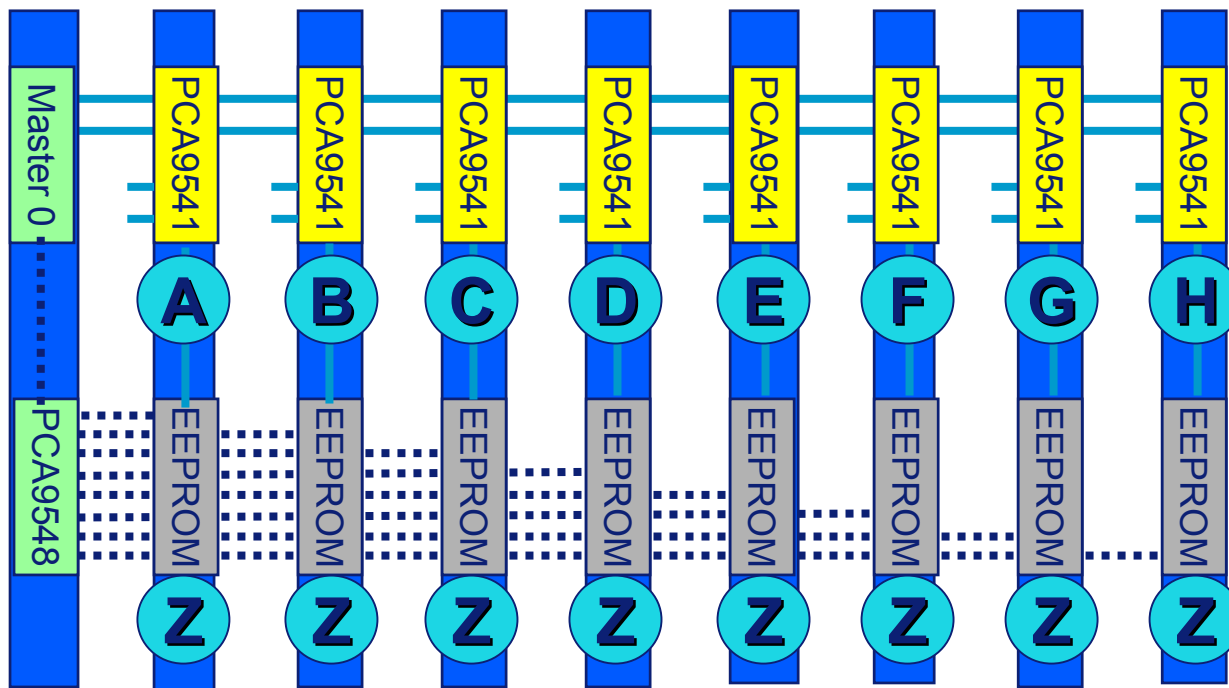
# PCA9541 – Shared Resources



Some masters may not be multi-master capable or some masters may not work well together and continually lock up the bus. The PCA9541 can be used to separate the masters, but still allow shared access to slave devices, such as Field Replaceable Unit (FRU) EEPROMs or temperature sensors such as is represented by Slave A0 and Slave B0.

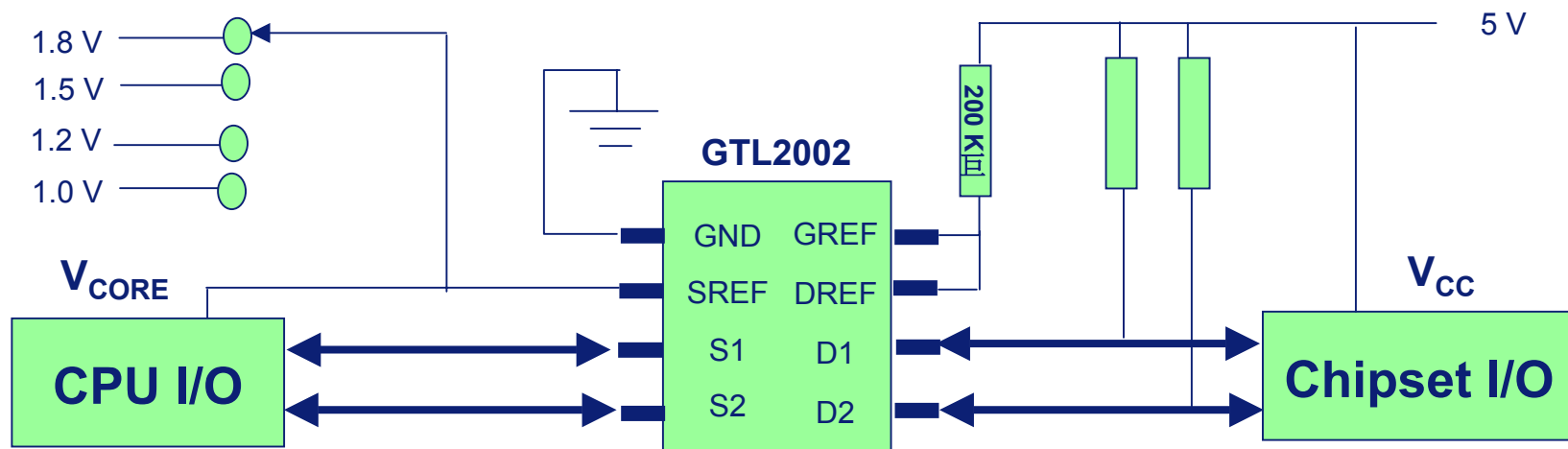
# PCA9541 – Gatekeeper Multiplexer

- The PCA9541/03 acts as the gatekeeper to each card that have identically I<sup>2</sup>C addressed EEPROMs. The master turns each uniquely addressed PCA9541/03 on (master 0) and off, one at a time, to communicate with the EEPROMs.



- The alternative is to use a PCA9548 to 1 to 8 multiplexer on the master card and then run 8 I<sup>2</sup>C buses, one to each EEPROM card. You use the same number of card pins but have 8 times the number of traces on the backplane.

# I<sup>2</sup>C Bus Bi-Directional Voltage Level Translation



- Voltage translation between any voltage from 1.0 V to 5.0 V
- Bi-directional with no direction pin
- Reference voltage clamps the input voltage with low propagation delay
- Application Note AN10145

- **GTL2000 22-Bit**
- **GTL2002 2-Bit**
- **GTL2010 10-Bit**

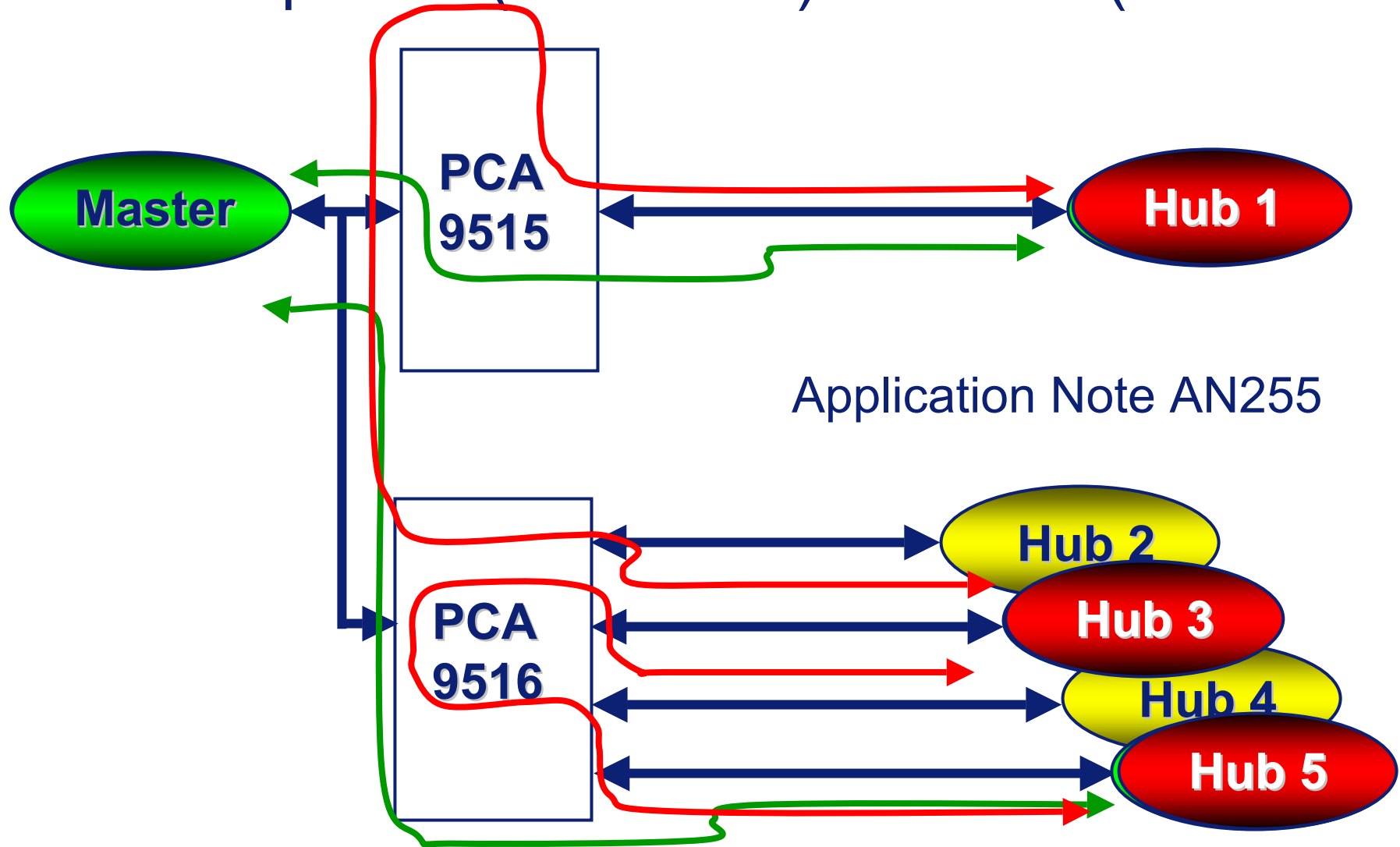


# I<sup>2</sup>C Multiplexers and Switches

Device	Multiplexer (In/Out)	Switch (In/Out)	Features			Packages				
			# of Addresses	Interrupt (In/Out)	Hardware RESET	Pin Count	SO (Narrow)	SO (wide)	TSSOP	HVQFN
PCA9540	1-2		1			8	D		DP	
PCA9541	2-1		16	1-2	✓	16	D		PW	BS
PCA9542	1-2		8	2-1		14	D		PW	
PCA9543		1-2	4	2-1	✓	14	D		PW	
PCA9544	1-4		8	4-1		20		D	PW	BS
PCA9545		1-4	4	4-1	✓	20		D	PW	BS
PCA9546		1-4	8		✓	16	D		PW	BS
PCA9548		1-8	8		✓	24		D	PW	BS

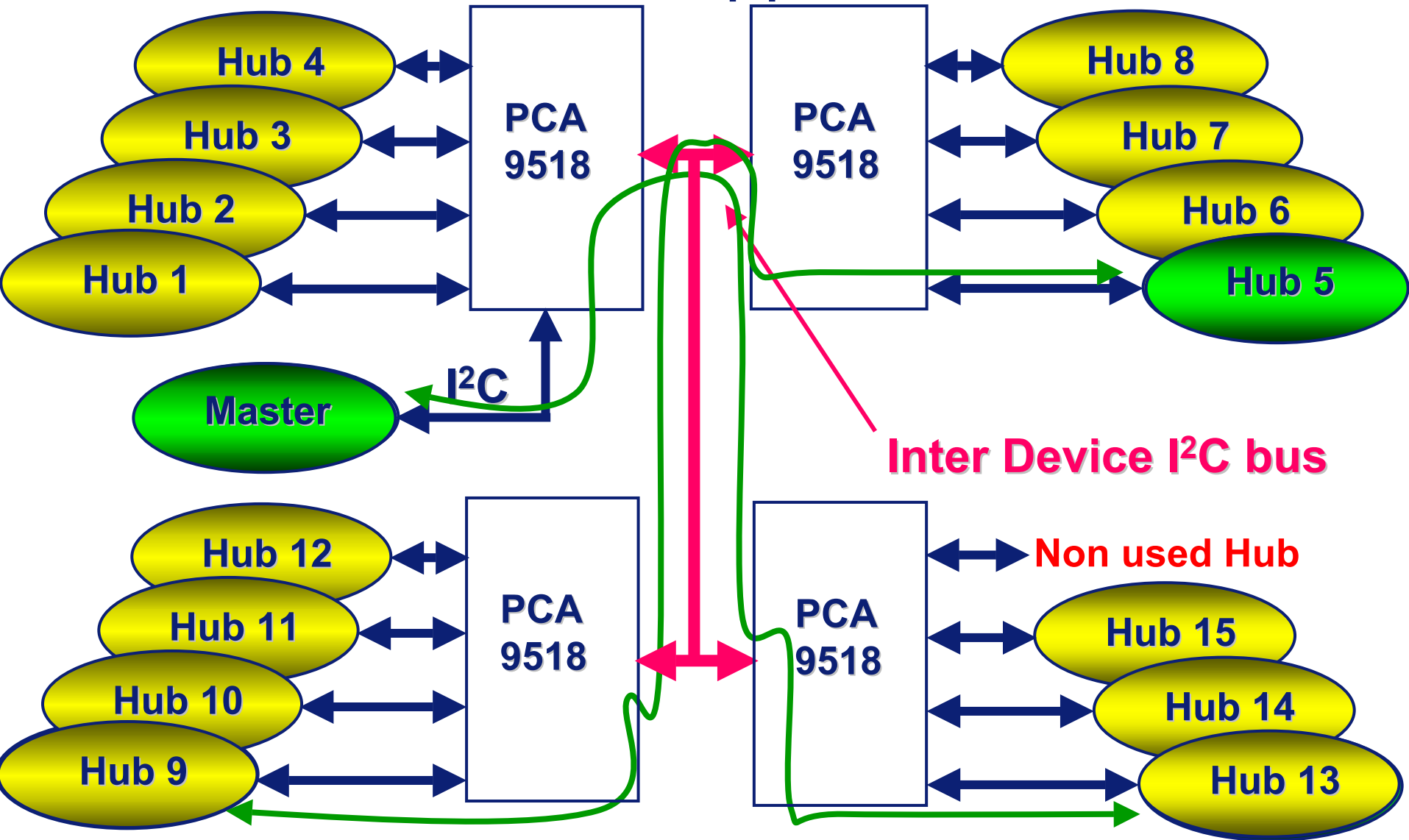
# Bus Buffers

# I<sup>2</sup>C Bus repeater (PCA9515) and Hub (PCA9516)



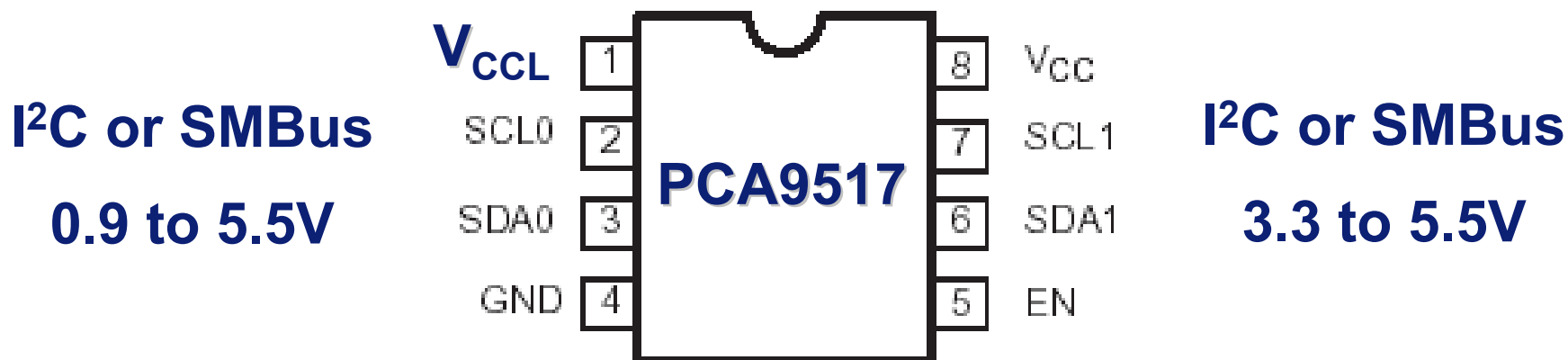
PCA9515 and PCA9516 were designed to isolate up to 400 pF on each segment and uses an offset  $V_{OL}$  to allow bi-directional signaling without use of a direction pin. They were not designed to operate on the same bus since a low signal is not passed through two devices.

# PCA9518 Applications



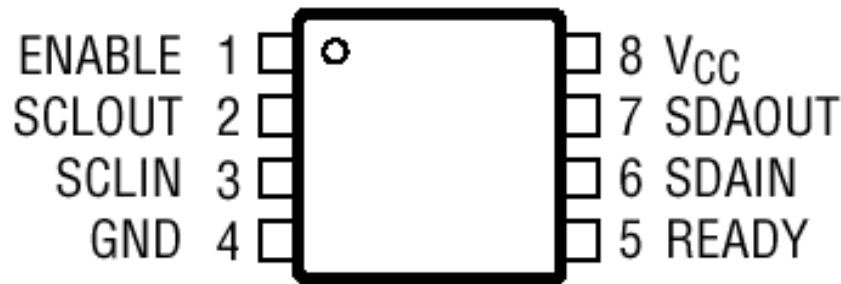
The PCA9518 was design to allow expansion to an unlimited number of segments of 400 pF each.

# Level Translation I<sup>2</sup>C Bus Buffer



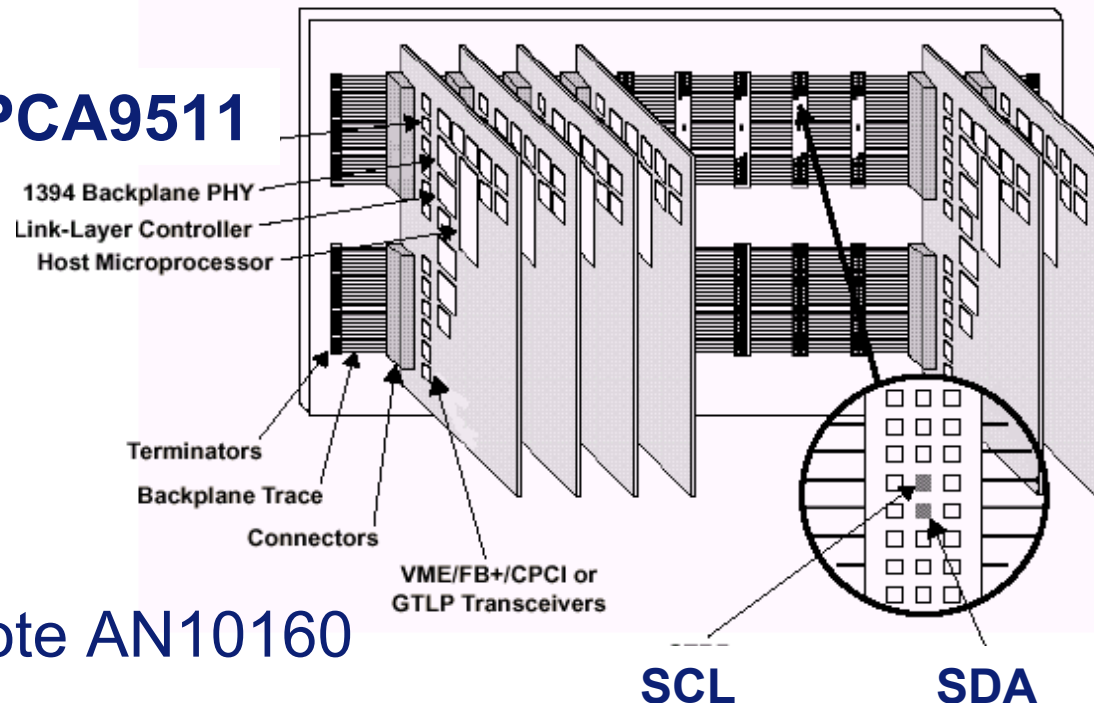
- Isolates capacitance allowing 400pF on each side of the device
- Enable/disable pin allows isolation of bus
- Dual V<sub>CC</sub>s allow voltage translation with optimum noise margin on the low voltage side
- Drop in replacement for the PCA9515

# I<sup>2</sup>C Hot Swap Bus Buffer



- Isolate capacitance
- Stop and Idle detect
- SDA/SCL Precharge
- Rise Time Accelerators

## PCA9511



Application Note AN10160

# I<sup>2</sup>C Hot Swap Bus Buffer

Feature	PCA9510	PCA9511	PCA9513	PCA9514		PCA9512
Alternate source to Linear Tech LTC4300-1ISM8	Similar	Yes	Similar	Similar		-
Alternate source to Linear Tech LTC4300-2ISM8	-	-	-	-		Yes
Idle Detect	Yes	Yes	Yes	Yes		Yes
High Impedance SDA, SCL pins for Vcc = 0V	Yes	Yes	Yes	Yes		Yes
Rise Time Accelerator Circuitry on all SDA and SCL lines	No	Yes	Yes	Yes		Yes
Rise Time Accelerator Circuitry Hardware Enable Pin	-	-	-	-		Yes
Rise Time Accelerator threshold 0.8 V vs 0.6 V improves noise margin	-	-	Yes	Yes		-
Low Icc chip disable < 1 uA	Yes	Yes	Yes	Yes		No
Ready Open Drain Output	Yes	Yes	Yes	Yes		No
Separate Vccs to support 5 V to 3.3 V level translation	-	-	-	-		
1V Precharge on all SDA and SCL Lines	bus side	Yes	No	No		Yes
92 uA Current Source on SCLIN and SDAIN for PICMG applications	-	-	Yes	-		-
Improve acknowledge and clock stretching behavior	Yes	Yes	Yes	Yes		Yes

# Intelligent Platform Management Interface

- Intel initiative in conjunction with hp, NEC and Dell to standardize the maintenance and monitoring of non hot swap server applications.
- Consists of three specifications:
  - Intelligent Platform Management Interface (IPMI) for software extensions
  - Intelligent Platform Management Bus (IPMB) for intra-chassis (inside the box) extensions and is I<sup>2</sup>C based
  - Inter Chassis Management Bus (ICMB) for inter-chassis (outside of the box) extensions
- Needed since as the complexity of systems increase, MTBF decreases
- Defines a standardized, abstracted, message-based interface to intelligent platform management hardware.
- Defines standardized records for describing platform management devices and their characteristics.
- Provides a self monitoring capability increasing reliability of the systems
- **More information – [www.intel.com/design/servers/ipmi/ipmi.htm](http://www.intel.com/design/servers/ipmi/ipmi.htm)**



# CompactPCI, AdvancedTCA and VME use IPMI

Known as	Specification	Based on	Comments
cPCI	PICMG 2.0	NA	No IPMB
cPCI	PICMG 2.9	IPMI 1.5	Single hot swap IPMB optional
AdvancedTCA	PICMG 3.x	IPMI 1.5	Dual redundant hot swap IPMB mandatory

- IPMI is used as the basis for the management and monitoring of these hot swap telecom applications

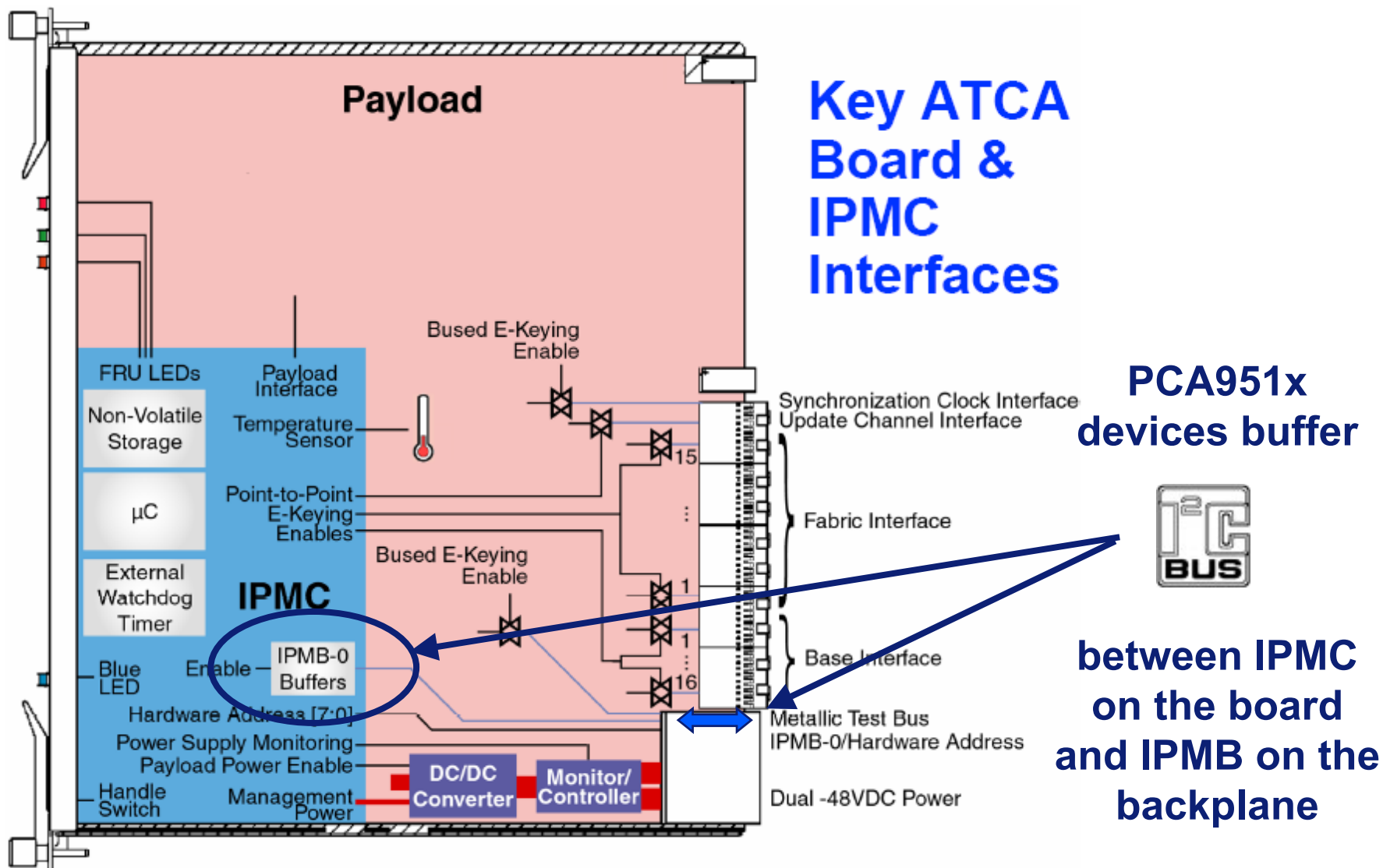
- PICMG 2.0: CompactPCI Core
- PICMG 2.9: System Management
- PICMG 3.0: AdvancedTCA Core
  - 3.1 Ethernet Star (1000BX and XAUI)
  - 3.2 InfiniBand® Star & Mesh
  - 3.3 StarFabric
  - 3.4 PCI Express
- VME will use PICMG 2.9 specifications

These systems will use the PCA9510/11/12/13/14 to help buffer capacitance and provide hot swap protection.

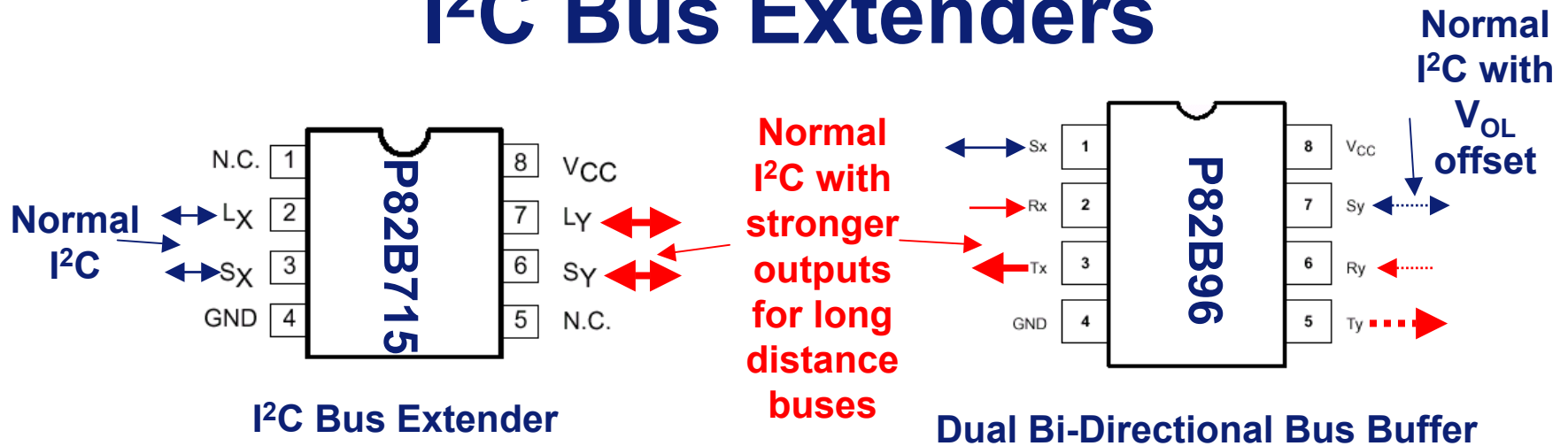
- **AdvancedTCA tutorial >**

[http://www.picmg.org/advancedTCA\\_Tutorial\\_0503.stm](http://www.picmg.org/advancedTCA_Tutorial_0503.stm)

# Bus Buffers used on every ATCA board!



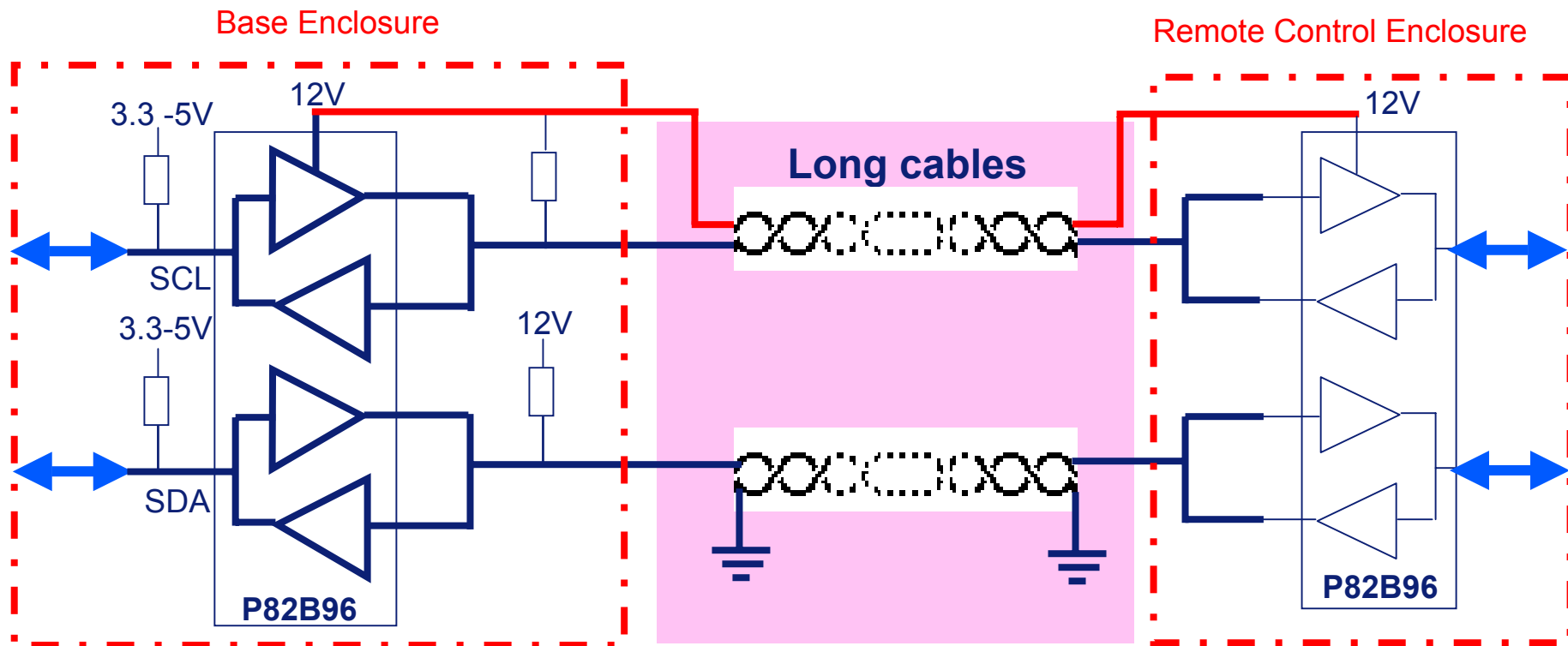
# I<sup>2</sup>C Bus Extenders



## KEY POINTS

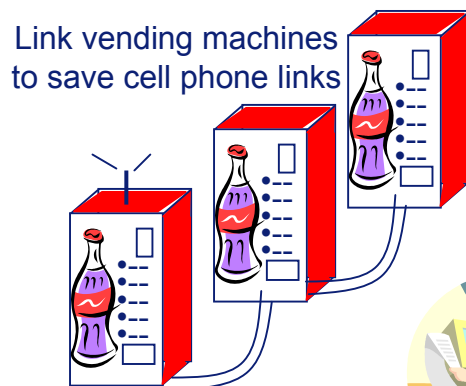
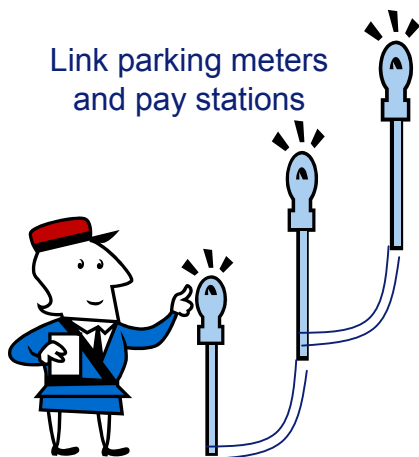
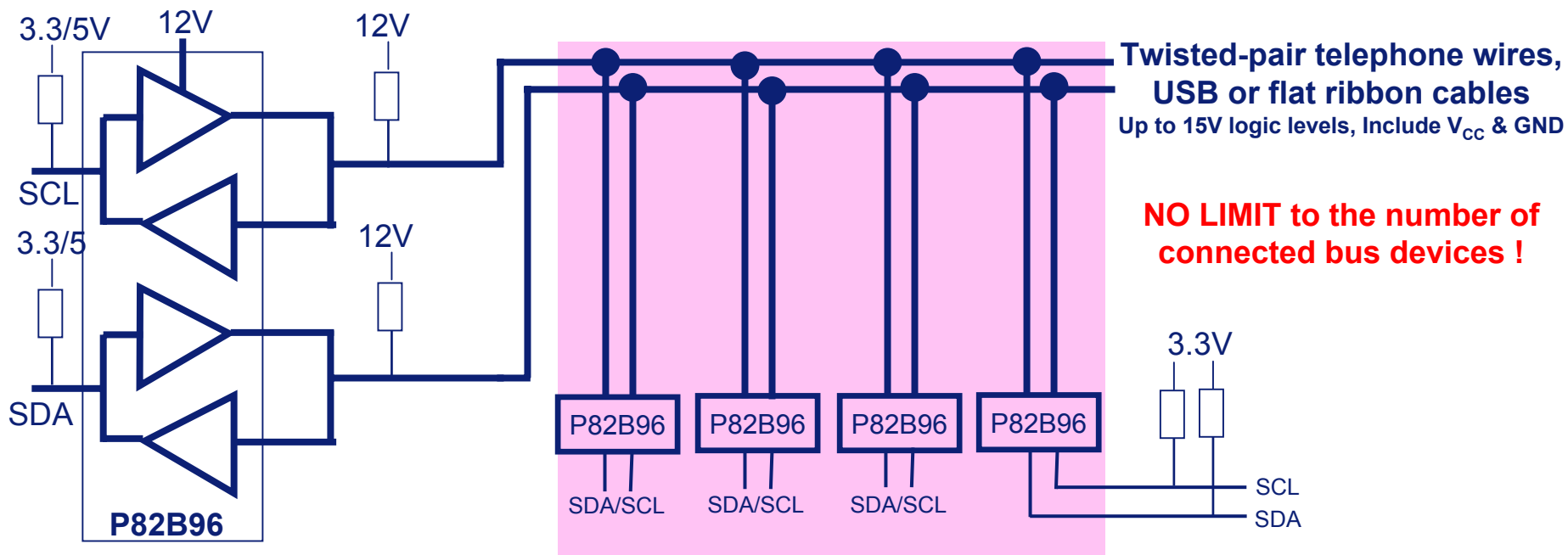
- High drive outputs are used to extend the reach of the I<sup>2</sup>C bus and exceed the 400 pF/system limit. Can be used in 400 kHz systems.
- Possible distances range from 50 meters at 85 kHz to 1km at 31 kHz over twisted-pair phone cable.
- P82B96 has split high drive outputs allowing differential transmission or Opto-isolation of the I<sup>2</sup>C Bus.
- The 715 doesn't isolate capacitance beyond 3000 pF but doesn't use offset V<sub>OL</sub> like the 96 so it is better for V<sub>OL</sub> sensitive applications.
- See Application Note AN255 for more details.

# Driving I<sup>2</sup>C bus signals long distances



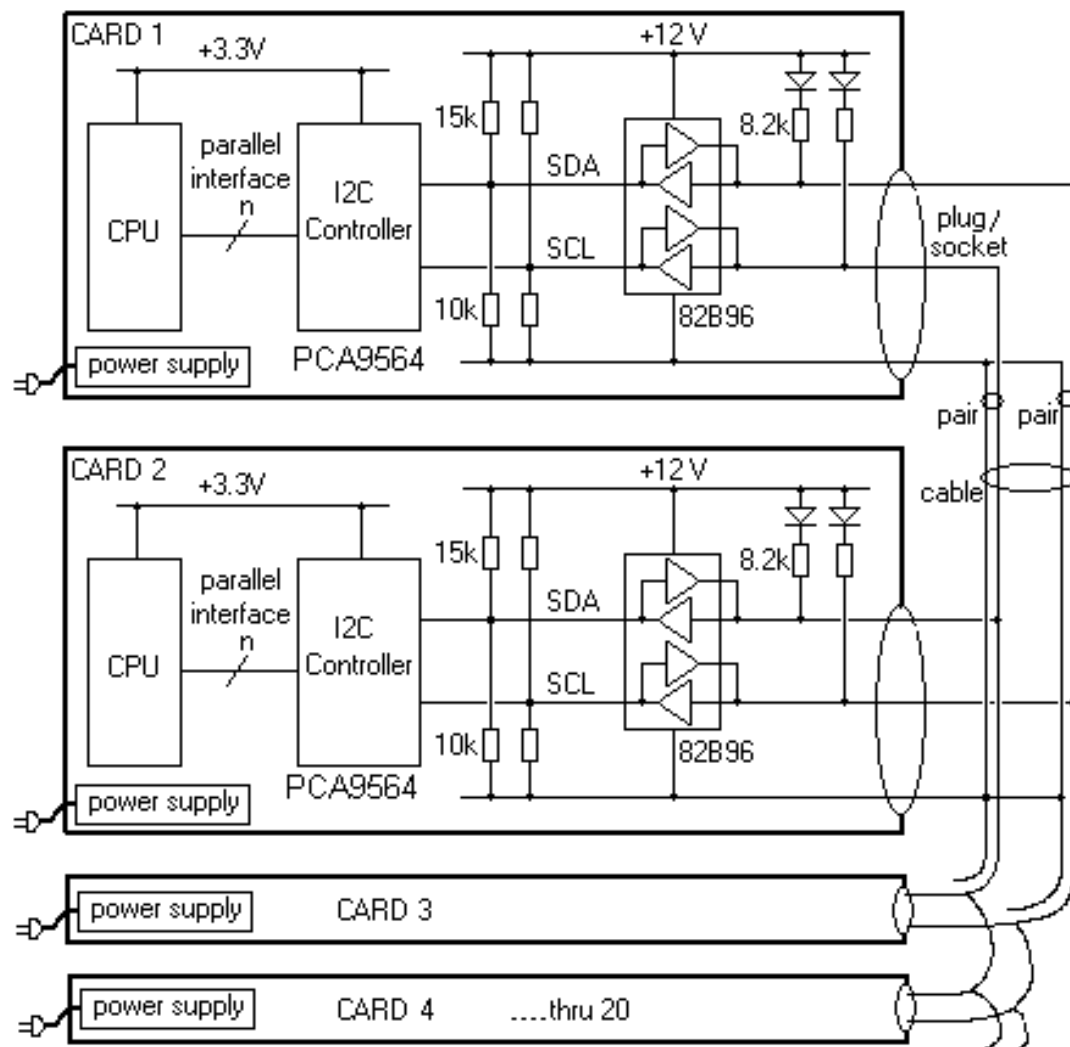
- Normal I<sup>2</sup>C logic levels (3.3 or 5 V)
- I<sup>2</sup>C currents (3mA)
- Conventional CMOS logic levels (2-15V)
- Higher current option, up to 30mA static sink
- Normal I<sup>2</sup>C logic levels (3.3 or 5 V)
- I<sup>2</sup>C currents (3mA)

## Changing I<sup>2</sup>C bus signals for multi-point applications!



- Factory automation
- Access/alarm systems
- Video, LCD & LED display signs
- Hotel/motel management systems
- Monitor emergency lighting/exit signs

## Changing I<sup>2</sup>C bus signals for multi-point applications!

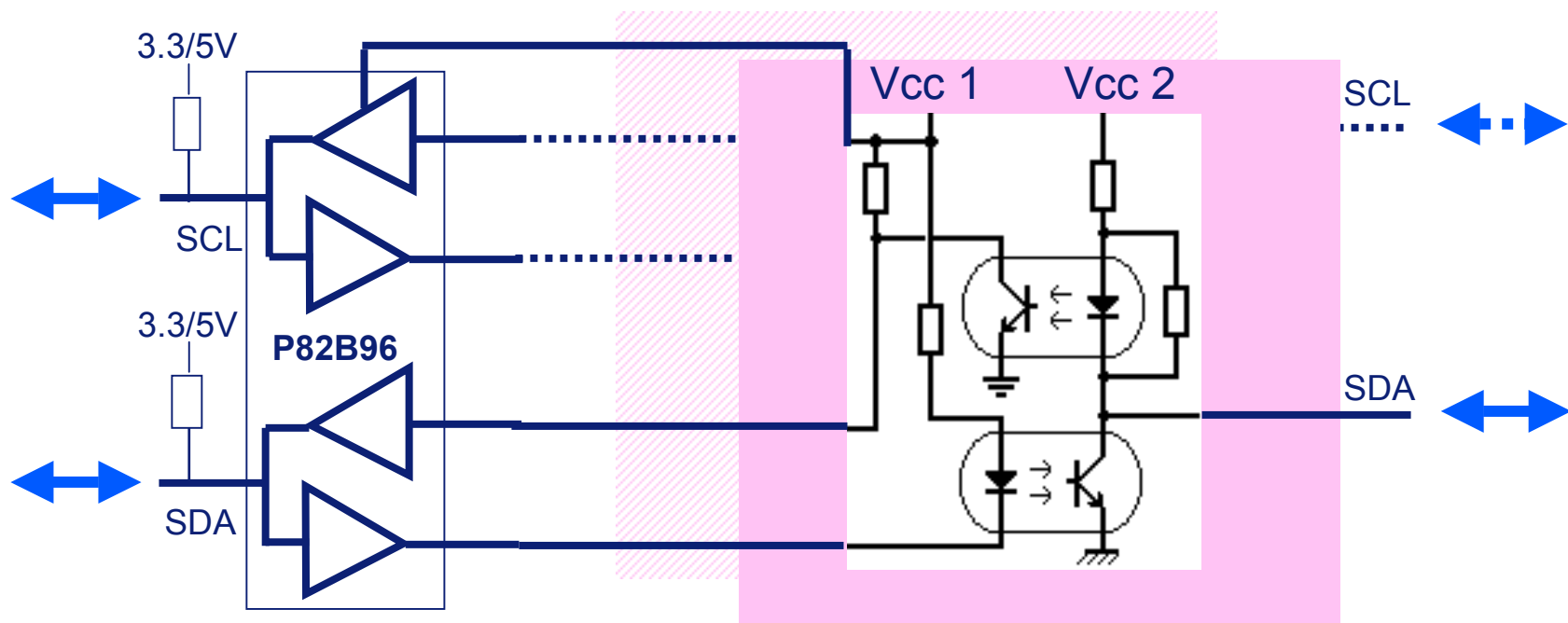


**Twisted-pair  
telephone wires,  
USB or flat ribbon  
cables  
Up to 15V logic  
levels, Include  $V_{CC}$  &  
GND**

**NO LIMIT to the  
number of  
connected bus  
devices !**

**Connect servers  
together**

# Changing I<sup>2</sup>C bus signals for Opto-isolation



- Low cost Optos can be directly driven (10-30mA)

4N36 Optos for ~5kHz  
 6N137 for 100kHz  
 HCPL-060L for 400 kHz

- Controlling equipment on phone lines
- AC Mains switches, lamp dimmers, power supplies
- Isolating medical or industrial equipment

# I<sup>2</sup>C Bus Buffers

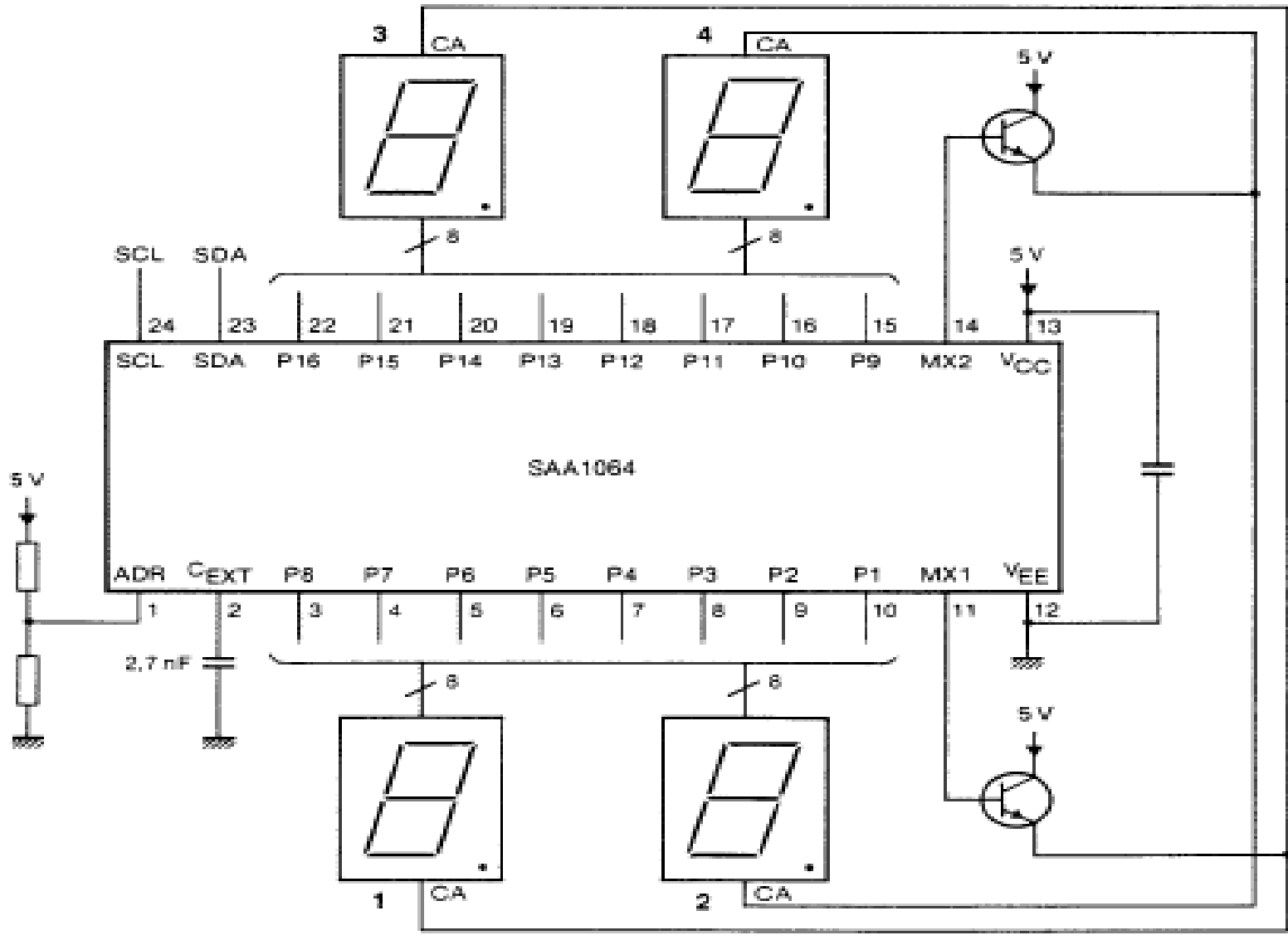
Product	Usage					
	Bus Buffer	Long Distance Bus	Bus Isolation/ Multiplexing	Voltage Translation	Multi-Point Distribution	Opto-Electrical Isolation
<b>P82B715</b>	3000pF	✓✓✓			✓✓✓	
<b>P82B96</b>	4000pF	✓✓✓	✓	✓✓✓	✓✓✓	✓✓✓
<b>PCA9511</b>	800pF	✓	✓✓	✓	✓✓✓	
<b>PCA9512</b>	800pF	✓	✓	✓✓	✓✓✓	
<b>PCA9513</b>	800pF	✓	✓✓	✓	✓✓✓	
<b>PCA9514</b>	800pF	✓	✓✓	✓	✓✓✓	
<b>PCA9515</b>	800pF		✓✓	✓		
<b>PCA9516</b>	2000pF		✓✓✓	✓		
<b>PCA9518</b>	2000pF x n		✓✓✓	✓		

Usage Legend: ✓ = Good, ✓✓ = Better, ✓✓✓ = Best



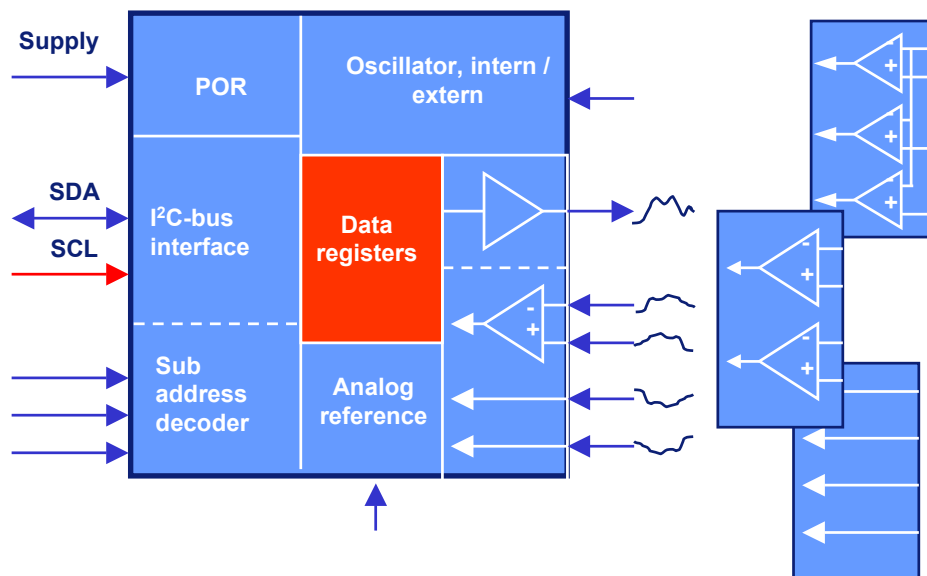
# Segment Drivers

# SAA1064 Driving Four 7 Segment plus Decimal



# A/D Converters

# Analog to Digital Converter



## KEY POINTS

- Converts signals from digital to analog and analog to digital

## FEATURES

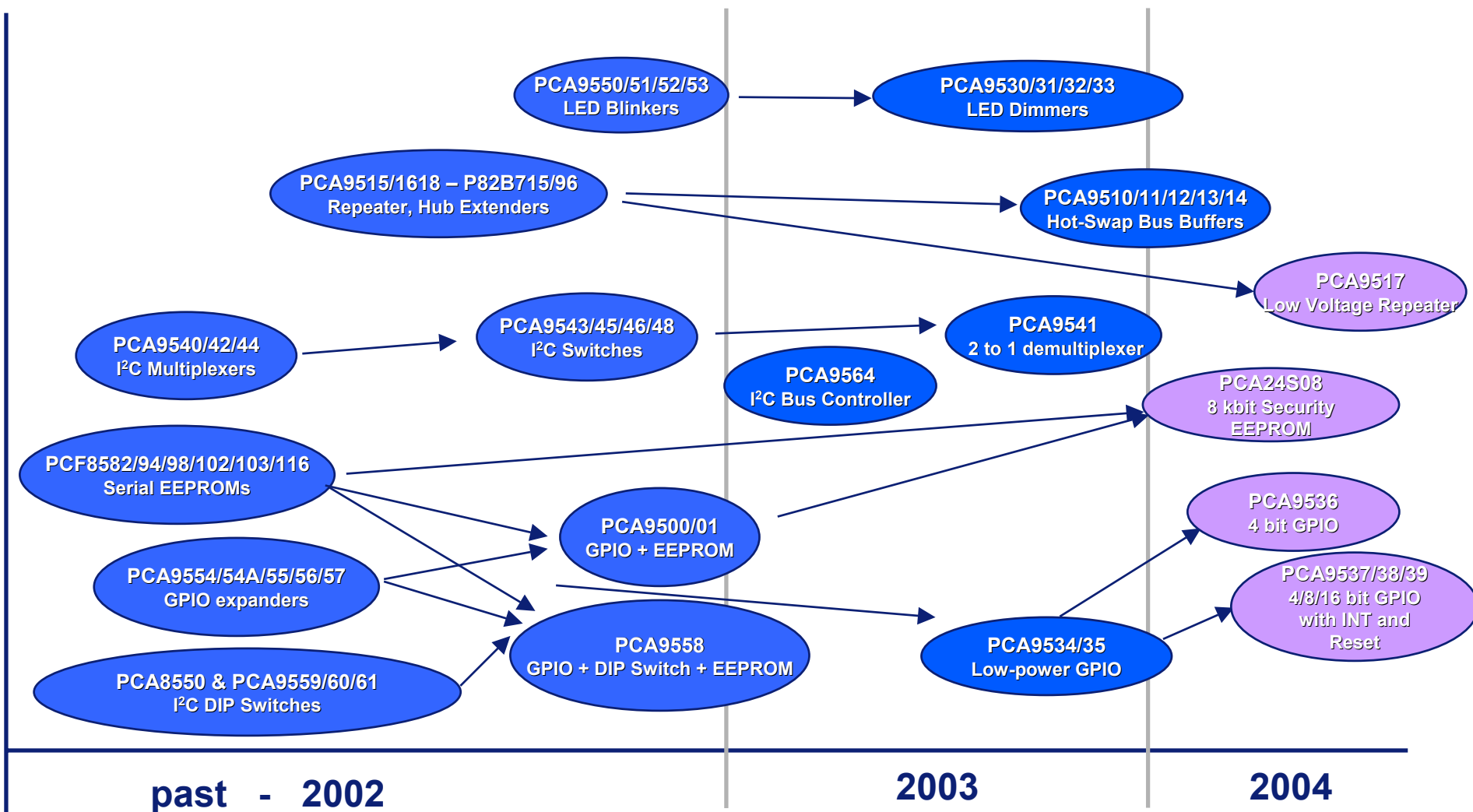
- 4 channel A to D
- 1 channel D to A
- Internal oscillator
- Power On Reset (POR)

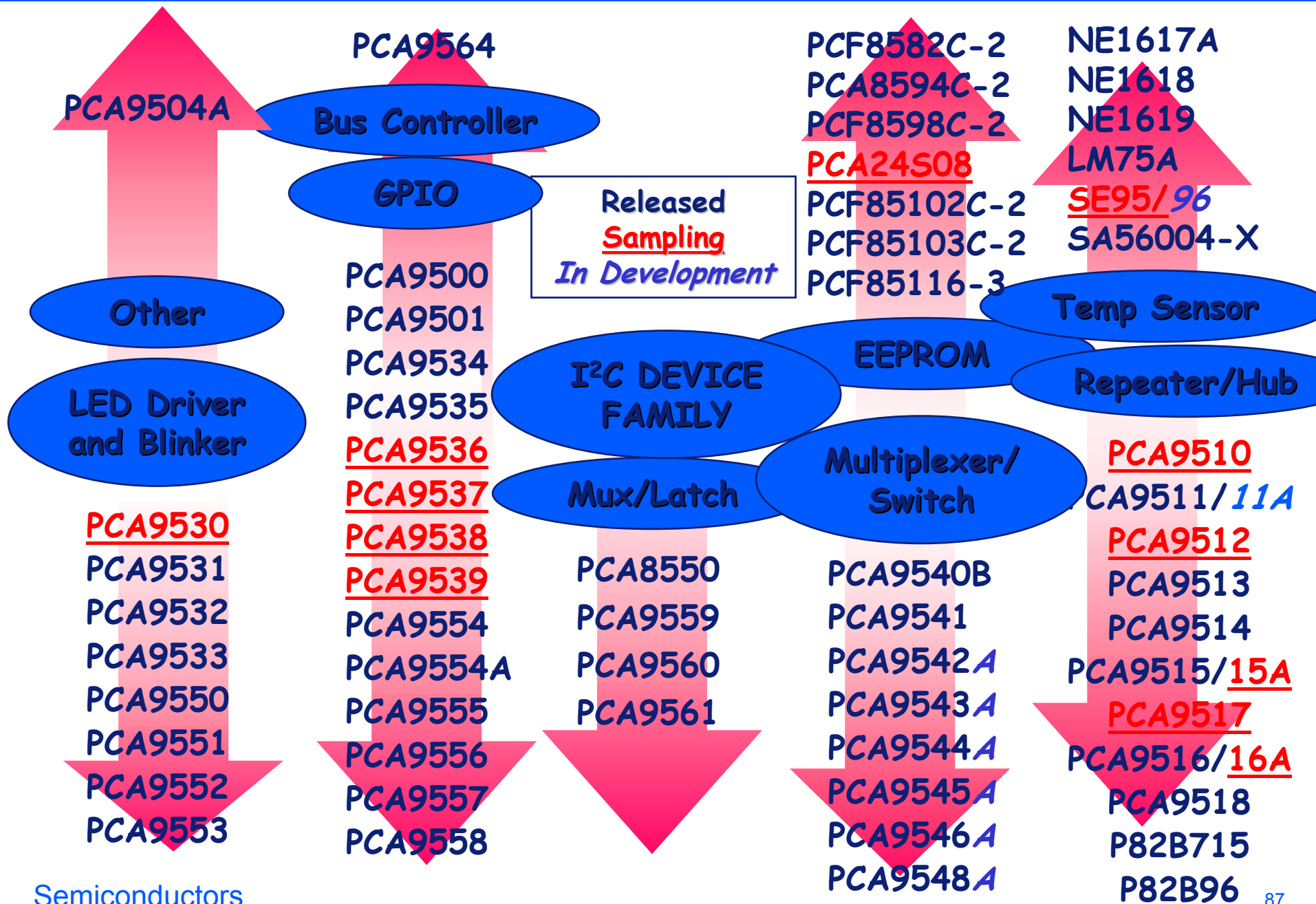
	Voltage range	Max I²C freq	Resolution
PCF8591	2.5 - 5.5V w/5V tolerance	100 kHz	8-bit

# Roadmap

# I<sup>2</sup>C Logic Roadmap

Available Development Roadmap





# Package Roadmap

Single Bit

MicroPkg  
PicoPkg

8 Bit



SO SSOP TSSOP



DQFN

16 Bit

SSOP TSSOP TVSOP

HVQFN VFBGA

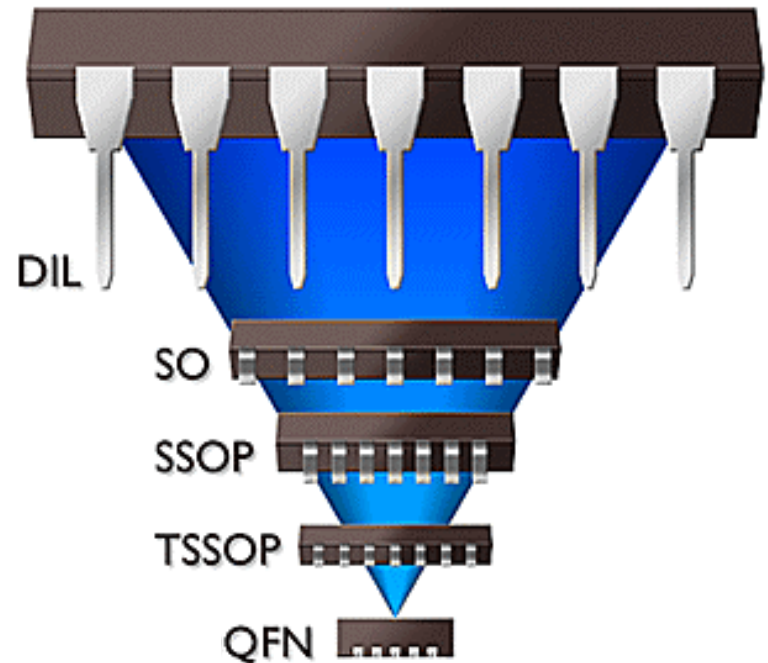
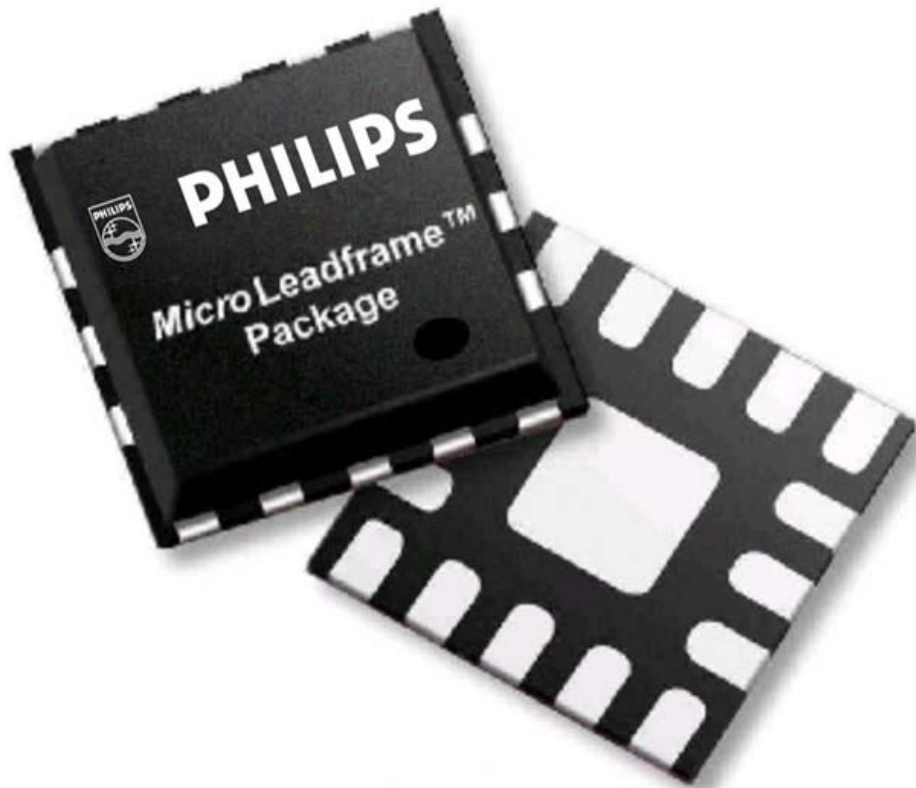
32 Bit

LFBGA

I<sup>2</sup>C Logic devices are offered in  
SO, SSOP, TSSOP and HVQFN



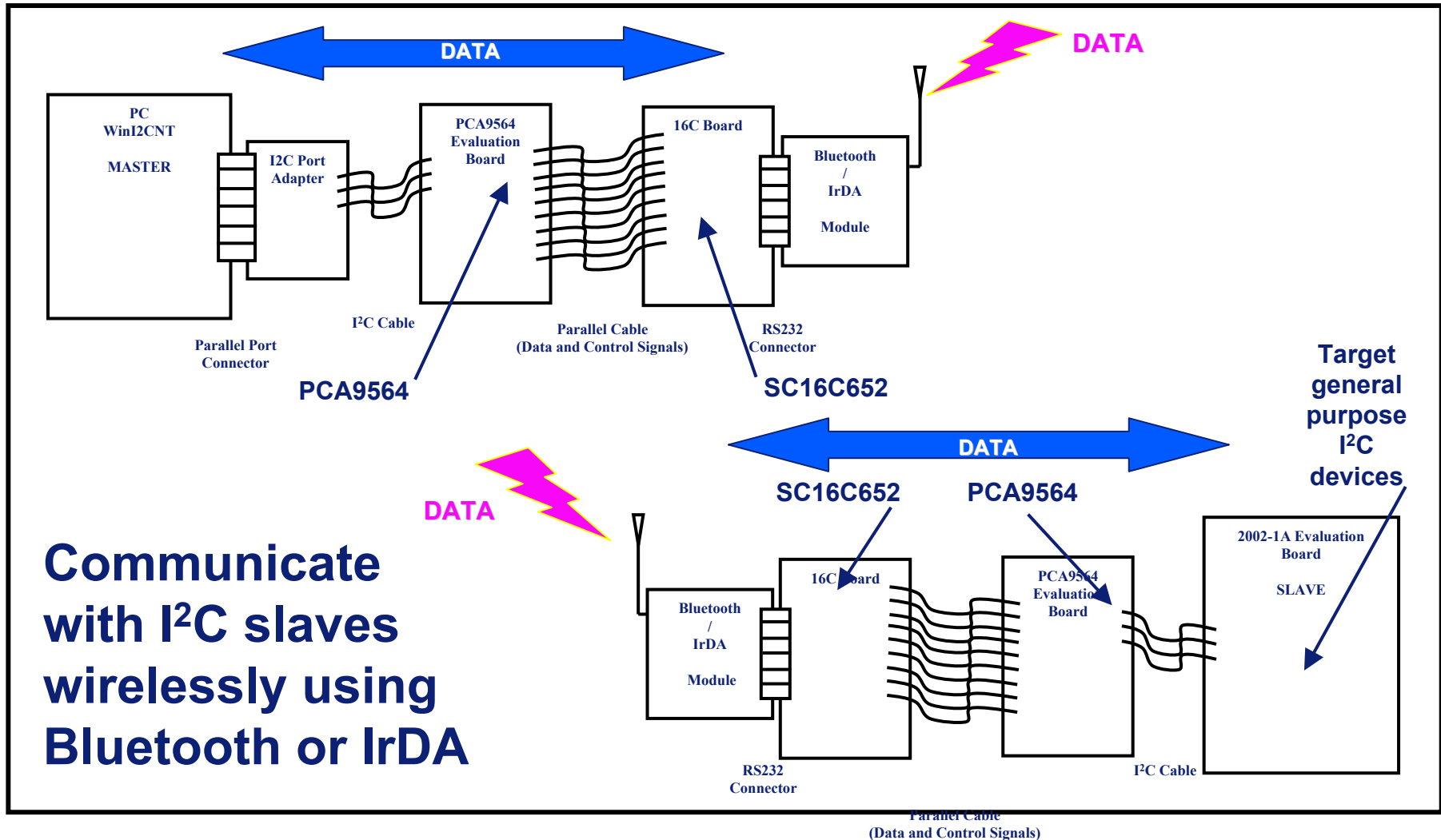
# MLP/HVQFN



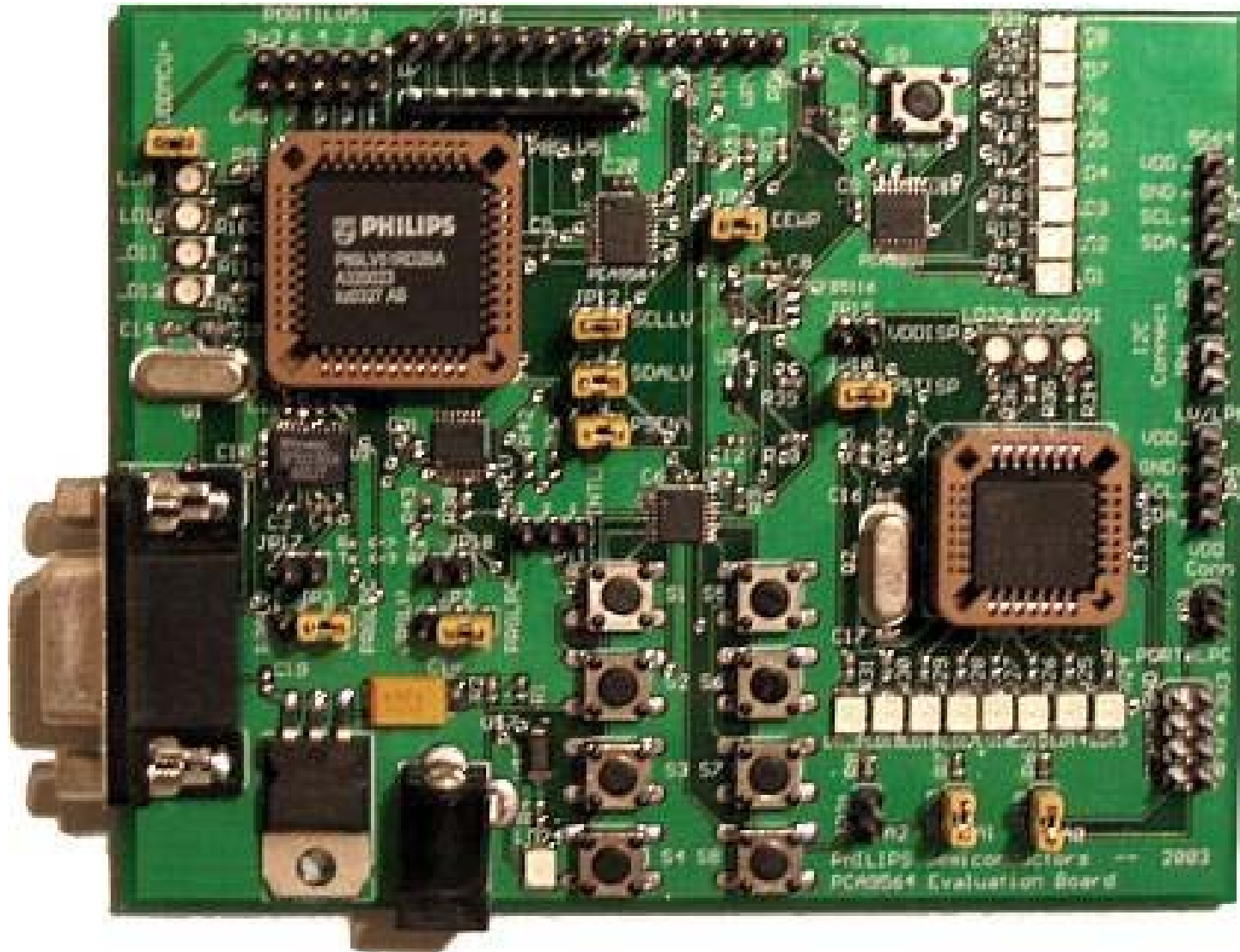
New **H**eat Sink **V**ery Thin **Q**uad **F**lat pack **N**o Lead  
Packages are 75% Smaller than TSSOP

# Support Material

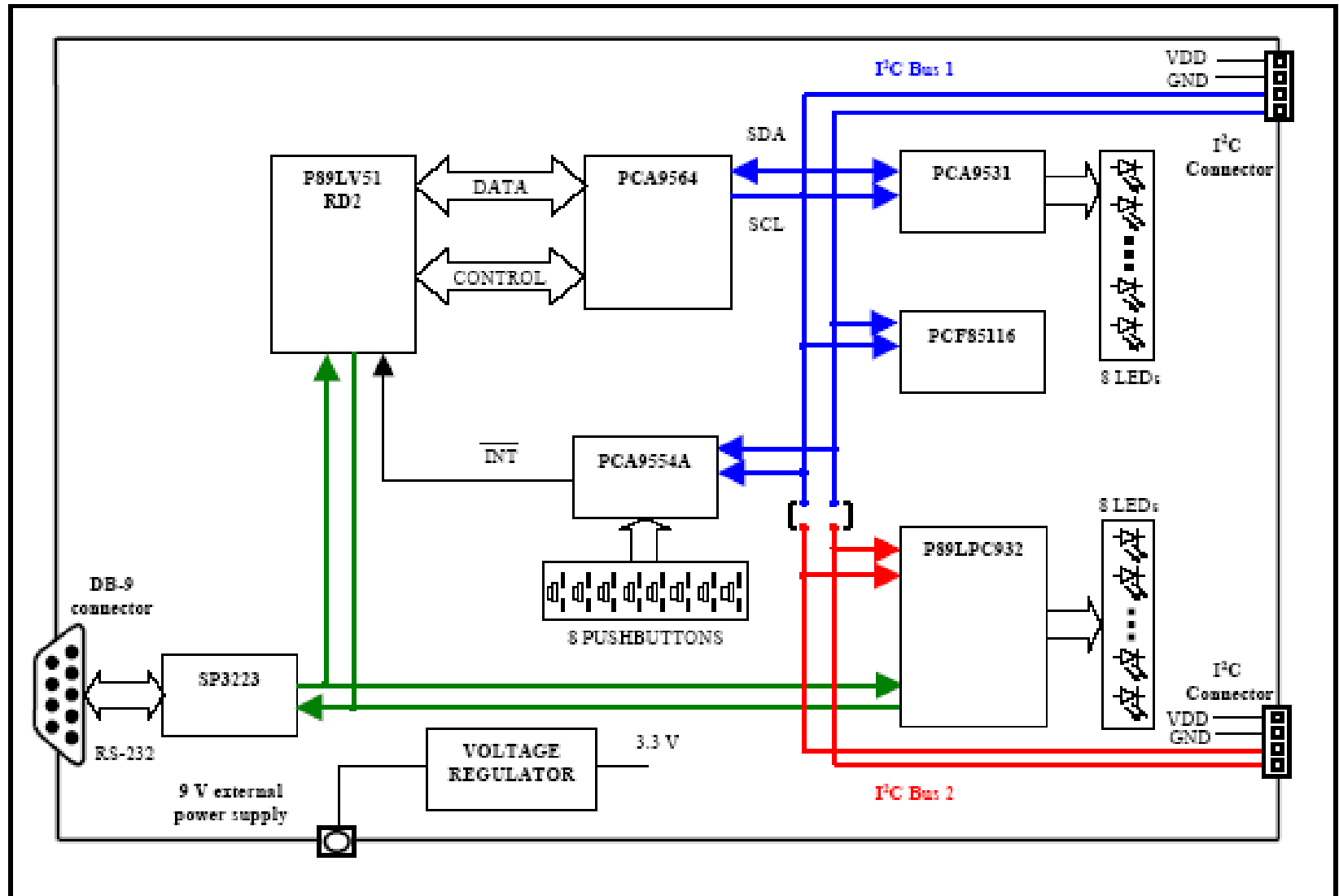
# Combined I<sup>2</sup>C and UART Demo Board



# PCA9564 Demo Board Picture



# PCA9564 Demo Board Layout



# I2C 2002-1A Evaluation Board Kit



Provide easy to use, PC based system to play with the I<sup>2</sup>C devices and learn how they operate.

## FEATURES

- Converts Personal Computer parallel port to I<sup>2</sup>C bus master
- Simple to use graphical interface for I<sup>2</sup>C commands with new expert mode
- Win-I2CNT software compatible with Windows 95, 98, ME, NT, XP and 2000
- Order kits at [www.demoboard.com](http://www.demoboard.com)
- Support tools > <http://www.semiconductors.philips.com/buses/i2c/tools/index.html>

## PCA9551 LED Blinkers Win-I2CNT Interface Screen

The screenshot shows the 'Win-I2CNT - [PCA9551 8-bit LED Driver / Blinker]' window. It features a graphical interface for controlling the PCA9551 LED driver. The interface includes sections for PWM settings, register information, and LED control. Annotations highlight key features:

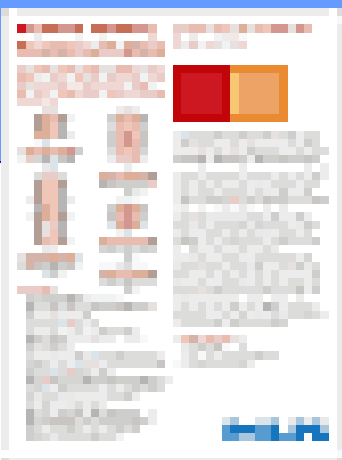
- Select LEDs mode:** Indicated by a red bracket on the right side of the window, pointing to the LED 1 and LED 0 status indicators.
- Device address CC for PCA9551:** A pink oval highlights the 'I2C Address' dropdown menu, which is set to '0xC0'.
- Write and Read Registers:** An orange oval highlights the 'Write All', 'Read Input Reg.', and 'Read All' buttons.
- Select blinking options:** A blue oval highlights the PWM 0 and PWM 1 settings, including Period and Duty Cycle sliders.
- Register information:** A green oval highlights the 'Registers (hex)' section, which displays various registers like Input Register, Frequency Prescaler 0, PWM Register 0, etc.

At the bottom of the window, there are buttons for 'Slow' and '38 KHz'.

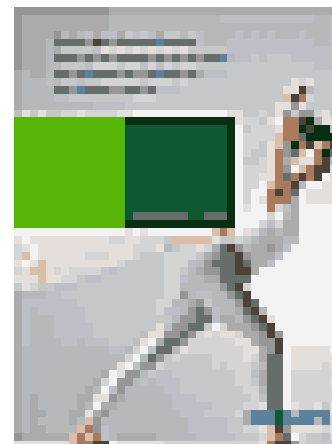
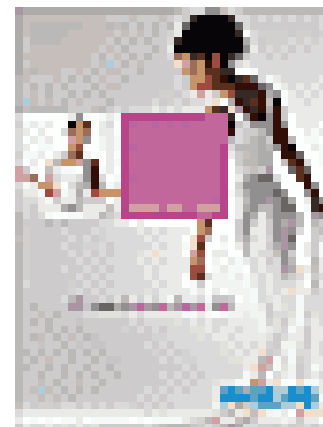
# I<sup>2</sup>C Product Flyers and Selection Guides



Provide  
overview of all  
the devices to



2003 I <sup>2</sup> C Selection Guide	Order Number: 9397 750 10591
2003 CBT Selection Guide	Order Number: 9397 750 10336
NE1617A/18/19	Order Number: 9397 750 07609
PCA8550	Order Number: 9397 750 04323
PCA9500/01	Order Number: 9397 750 09897
PCA9504A	Order Number: 9397 750 08562
PCA9515/16	Order Number: 9397 750 08205
PCA9540/42/44	Order Number: 9397 750 06542
PCA954X	Order Number: 9397 750 09222
PCA9550/51/52	Order Number: 9397 750 09208
PCA9554/54A/55	Order Number: 9397 750 08924
PCA9556	Order Number: 9397 750 06812
PCA9558	Order Number: 9397 750 08211
PCA9559	Order Number: 9397 750 06813
PCA9560/61	Order Number: 9397 750 09206
PCF EEPROM	Order Number: 9397 750 09209
P82B96	Order Number: 9397 750 09084





# I<sup>2</sup>C Device Data Sheets, IBIS models Application Notes and Other Information

Product family  
descriptions  
line cards  
cross reference  
data sheets

Link to  
app notes  
models  
user guides  
PLL design  
software  
datasheets

Provide easy to  
access to all the up to  
date data sheets,  
application notes and  
modeling tools.

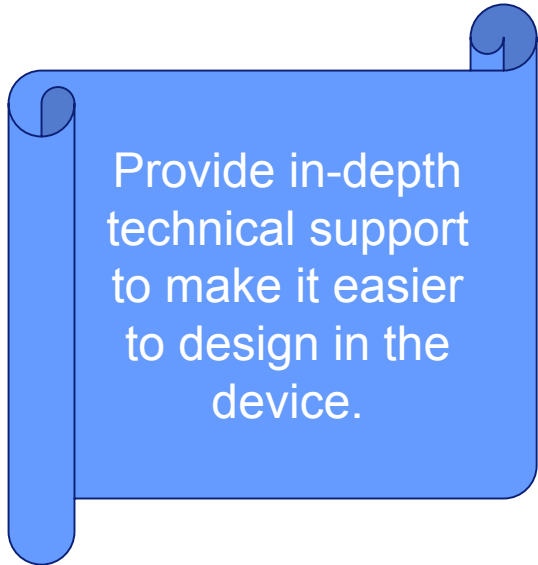
**[www.philipslogic.com/i2c](http://www.philipslogic.com/i2c) or  
[www.semiconductors.philips.com/i2c](http://www.semiconductors.philips.com/i2c)**



# Technical Support Information

## Application Notes

- AN250 PCA8550 4-Bit Multiplexed/1-Bit Latched 5-Bit I<sup>2</sup>C E2PROM
- AN255 I<sup>2</sup>C and SMBus Hubs, Buffers, and Repeaters
- AN444 P82B715 I<sup>2</sup>C Bus Buffer
- AN460 Introducing the P82B96 I<sup>2</sup>C Bus Buffer
- AN262 PCA954X Multiplexers and Switches
- AN264 I<sup>2</sup>C Devices for LED Display Control
- AN469 I<sup>2</sup>C I/O Port Selection
- AN10145 Bi-Directional Voltage Translators
- AN10146 I<sup>2</sup>C 2002-1A Evaluation Board
- AN10148 PCA9564 Bus Controller
- AN10149 PCA9564 Eval Board
- AN10160 I<sup>2</sup>C Hot Swap Bus Buffers \*\* (Jun)
- AN10216 I<sup>2</sup>C Manual



Provide in-depth technical support to make it easier to design in the device.

**Download from > [www.philipslogic.com/support/appnotes/](http://www.philipslogic.com/support/appnotes/)**

## I<sup>2</sup>C Sample Kit

The I<sup>2</sup>C Sample Kit consists of eight different I<sup>2</sup>C devices in tape inserted into the I<sup>2</sup>C Sample Kit box with an informative insert.




Devices include three each of the GTL2010PW, P82B96TD, PCA9551D, PCA9545D, PCA9555D, PCA9557D, PCA9515D and PCA9501D

Provide small quantity of free samples to make it easy to assemble and test your system.



Request I<sup>2</sup>C Sample Kit or individual samples from your Philips Sales Representative or directly from **I2C.Support at [philips.com](http://philips.com)**


# Easy Access to I<sup>2</sup>C Technical Help



Forum facilities

[? FAQ](#)
[Search](#)
[Profile](#)
[Logout \[ Steve Blozis \]](#)

## I2C discussion Forum


[new topic](#)
[Philips Semiconductors Forum Index -> I2C discussion Forum](#)

[Mark all topics read](#)


Topics	Replies	Author	Views	Last Post
 <a href="#">What is the required distance between SCL/SDA traces?</a>	1	<a href="#">Steve Blozis</a>	4	Wed Oct 29, 2003 8:24 pm <a href="#">Steve Blozis</a> →
 <a href="#">i2c 2002-1 Evaluation board</a>	1	<a href="#">juliana juhari</a>	19	Wed Oct 29, 2003 8:09 pm <a href="#">Steve Blozis</a> →

Three easy ways to ask technical questions and obtain answers

Access from > [www.semiconductors.philips.com/buses/i2c/](http://www.semiconductors.philips.com/buses/i2c/)

Communications

- PRODUCT PORTAL ▶
- PRODUCT SELECTOR ▶
- CONTACT ▶

 Features

- 5 channel, bi-directional buffer
- I<sup>2</sup>C-bus and SMBus compatible
- Active high individual repeater enable in
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching
- Accommodates standard mode and fast
- Powered-off high impedance I<sup>2</sup>C pins
- Operating supply voltage range of 3.0 V

**CONTACT link on every Product Information Page**

**Send e-mail directly to I2C.Support at [philips.com](mailto:I2C.Support@philips.com)**



[www.semiconductors.philips.com/i2c](http://www.semiconductors.philips.com/i2c)

[www.philipslogic.com/i2c](http://www.philipslogic.com/i2c)