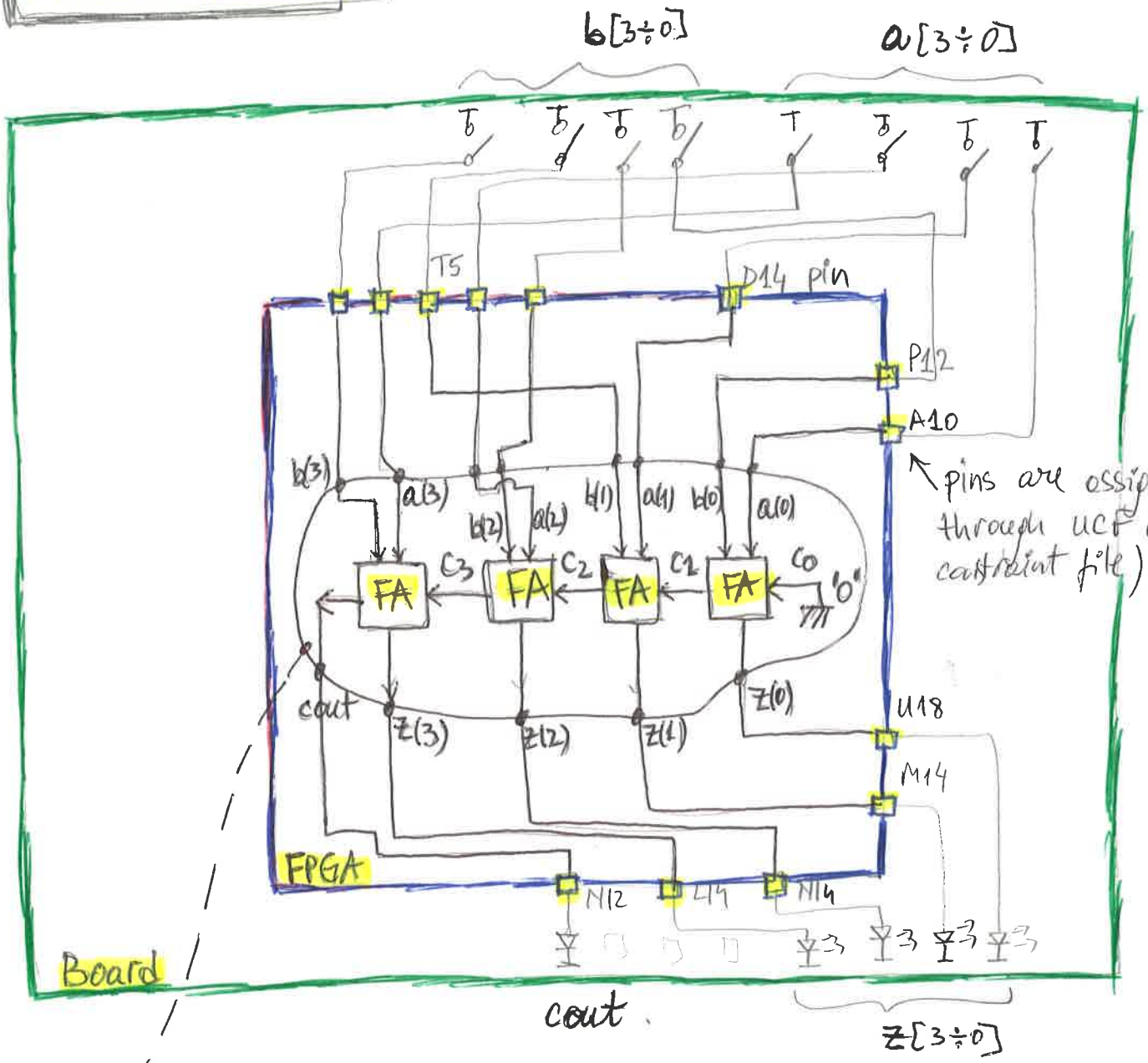
Introduction to VHDL

"fourbit_adder.vhd"



fourbit_adder.vhd

```
entity fourbit_adder is

end fourbit_adder;
```

design has one entity declaration

```
architecture MY_STRUCTURE of fourbit_adder is
    component, signals declarations
begin
    port maps, etc.
end MY_STRUCTURE;
```

entity has at least one architecture declarations!

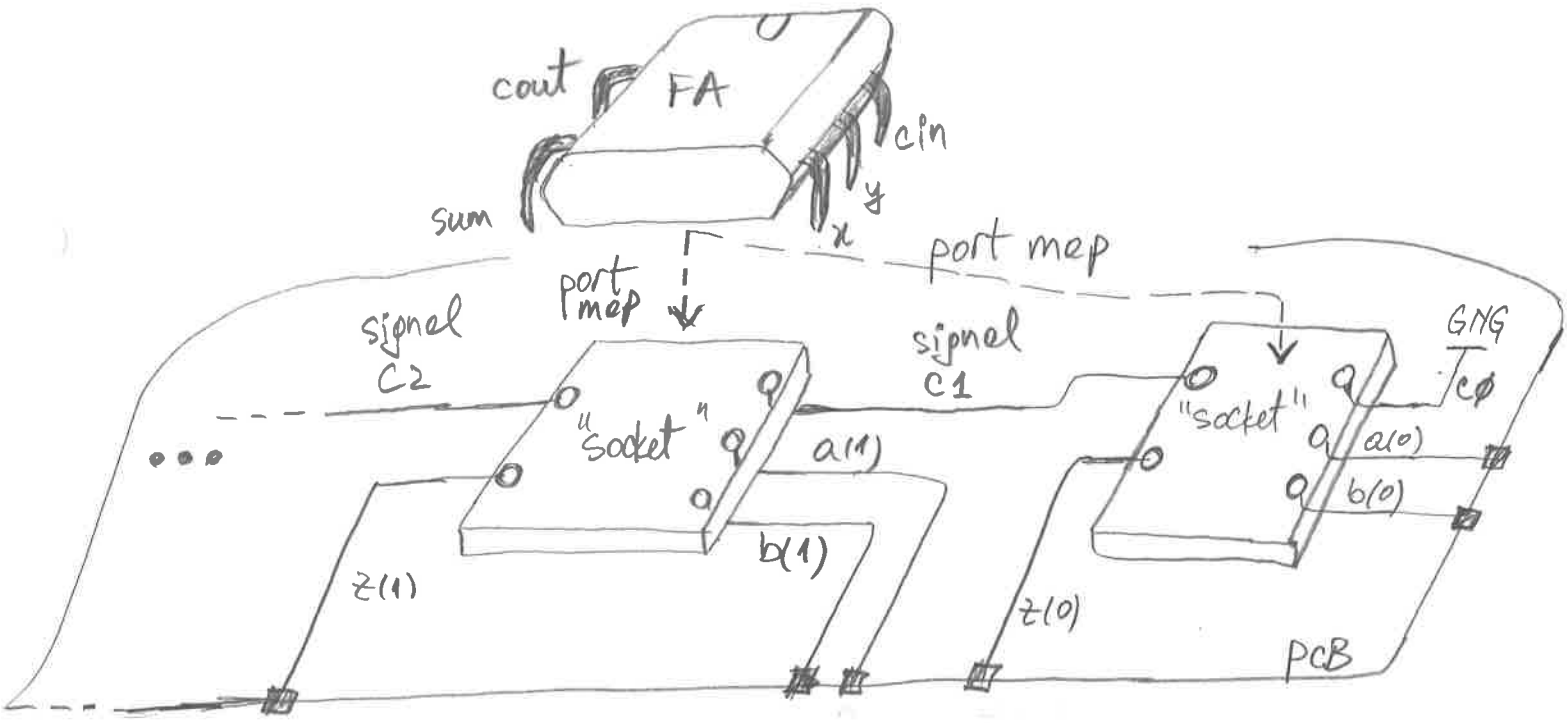
-- this is a comment! because it starts w/ "--"

- component declarations
- signal declarations ← use c0, c1 to port map.
- port map example:

b_adder0 : FULL_ADDER port map (a(0), b(0), c0, z(0), c1);

↑ declared and described in full_adder.vhd

- "visualization" of port map:



Next time:
- You must read VHDL introduction (see website of class)
- We'll discuss FSM's in VHDL