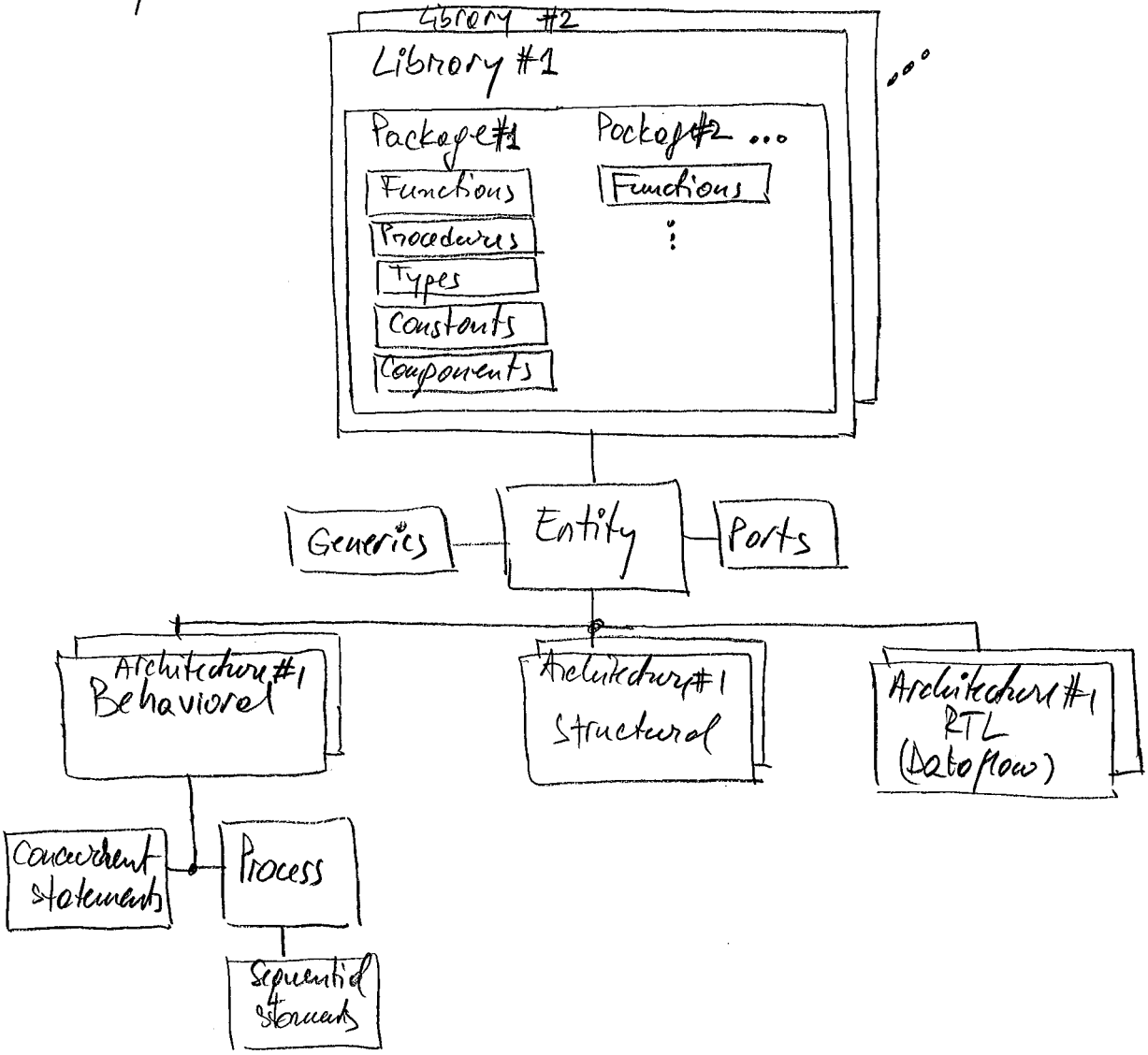
Packages & Libraries

- Extend the functionality of VHDL:
  - Define types, functions, components, overloaded operators.
- Standard libraries make portability easier!

```
library IEEE;
use IEEE.numeric_bit.all;
use IEEE.numeric_std.all;
```

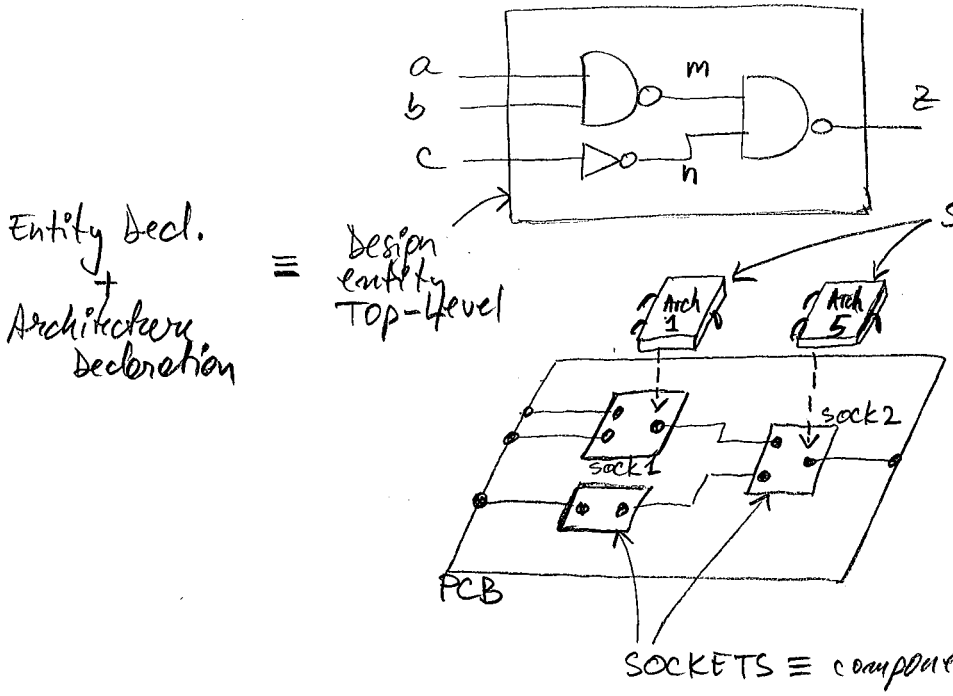
(library: IEEE; packages: numeric_bit, numeric_std)

- Anatomy of VHDL code:



Configurations

- Binds a component instance to an entity-architecture pair!



- Configuration:
  - selects one architecture from many architectures of one design entity for instantiation (specify which die goes in the package of the chip that will be plugged into socket on PCB!)

Example:

```
configuration CONFIG_1 of DESIGN_EXAMPLE_1 is
    for DES_EX_STRUCTURAL
        for SOCK1 use
            entity NAND2 (ARCH1)
        end for;
        for SOCK2 use
            entity NAND2 (ARCH5)
        end for;
    end for;
end CONFIG_1;
```