Manager-Worker Mandelbrot Fractal Generator

EECE-4740 Advanced VHDL Design and FPGAs, Instructor: Prof. Cris Ababei
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Abstract

- Use VHDL (VHSIC hardware description language) to design a Mandelbrot fractal generating algorithm
- Validate the design on an FPGA (field programmable gate array) chip: Cyclone IV E of Altera
- The fractal generating algorithm is composed of 22 workers and a single manager (the control block), which assigns pixels to the workers and stores their output
- Each worker runs in parallel with the control and the other workers

Hardware and Software

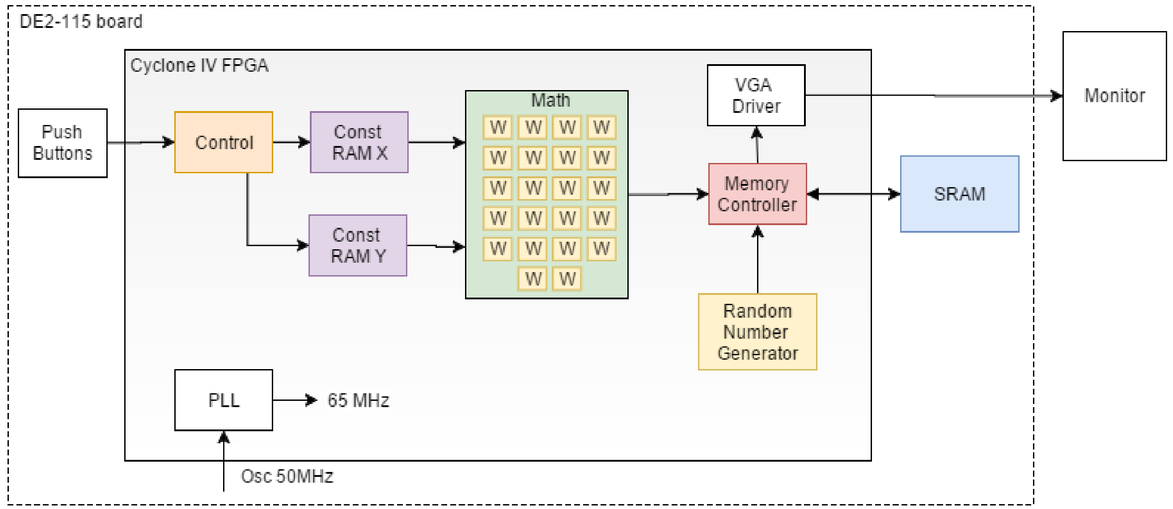
Hardware (HW):

- DE2-115 FPGA development board (made by Terasic); USD 300
- Cyclone IV E FPGA chip (located on board already, made by Altera); USD 12

Software (SW):

- Altera's Quartus Prime integrated design environment; Free
- Programming in VHDL language

Simplified Block Diagram



DE2-115 FPGA board

VGA monitor
1024x768 pixels

System in Action